LTA6051, LTA6052, LTA6054
250 MHz, High Slew Rate, RRO, CMOS Amplifiers

General Description

The LTA605x family is true single-supply voltage feedback operational amplifiers feature high speed performance with 250 MHz of small signal bandwidth and 190 V/µs slew rate. The products are specified for +3.3 V, +5 V, and ±5 V supplies, input common mode voltage range extends to 0.1 V below V_{S-} and 1 V from V_{S+}, and output voltage range extends to power rail, allowing wide dynamic range especially desirable in low voltage applications. The LTA605x also offer excellent signal quality of low distortion and fast settling time (13.5 ns to 0.1%), which make them ideal as buffers to single-supply ADCs.

Operating on supplies from +3.3 V to +12.6 V and dual supplies up to ±6.3 V, the LTA605x are ideal for a wide range of applications, from battery-operated systems with large bandwidth requirements to high speed systems where component density requires lower power dissipation. The single version LTA6051 device is available in micro-size SOT23-5L and SOIC-8L packages. The dual LTA6052 device is offered in MSOP-8L and SOIC-8L packages. The quad LTA6054 device is offered in SOIC-14L and TSSOP-14L packages.

Features and Benefits

- High Speed and Fast Settling on ±5 V
- 250 MHz, −3 dB bandwidth (G = +1)
- 190 V/µs slew rate
- 13.5 ns settling time to 0.1%
- Fully specified at +3.3 V, +5 V, and ±5 V Supplies
- Input Common Mode Voltage 0.1 V Beyond V_{S-}, 1 V from V_{S+}
- Output Voltage Swing from -4.6 V to +4.2 V (±5 V power supply)
- Output Short Circuit Current 210 mA
- Linear Output Current ± 130 mA
- Operating Temperature Range −40°C to +125°C

Applications

- Photodiode Amplification
- Video Buffer
- Active Filters
- Driving A/D Converters
- Motor Phase Current Sense
- Portable Equipment
- Battery-Powered Instrumentation

Table of Content

Ordering Information[1]

Part Number	Package Type	Package Size	Package Quantity	ECO Class[2]	Mark Code[3]
LTA6051XT5/R6	SOT23-5L	2.92 mm * 1.60 mm	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W51
LTA6051XS8/R8	SOIC-8L	4.90 mm * 3.92 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W6051
LTA6052XS8/R8	SOIC-8L	4.90 mm * 3.92 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W6052
LTA6052XV8/R6	MSOP-8L	3.00 mm * 3.00 mm	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W6052
LTA6054XS14/R5*	SOIC-14L	8.73 mm * 3.95 mm	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	W6054
LTA6054XT14/R6*	TSSOP-14L	4.96 mm * 4.40 mm	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W6054

* Preview Status (Not for MP stage, pls contact with us if you have request)

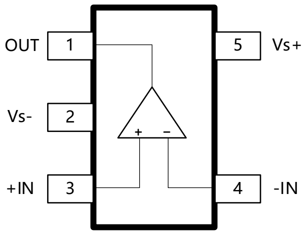
(1) Please contact to your Linearin representative for the latest availability information and product content details.

(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

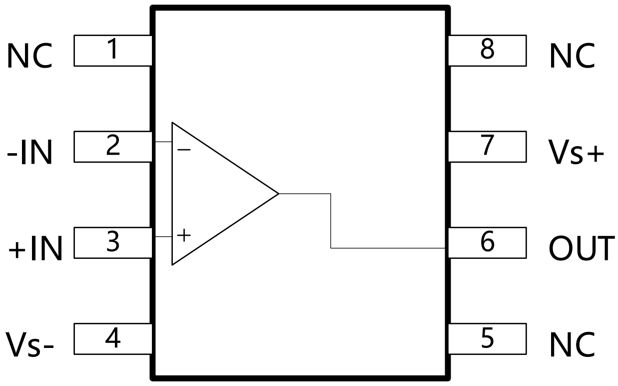
(3) There may be multiple device markings, a varied marking character of “x” , or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Pin Configuration (Top View)

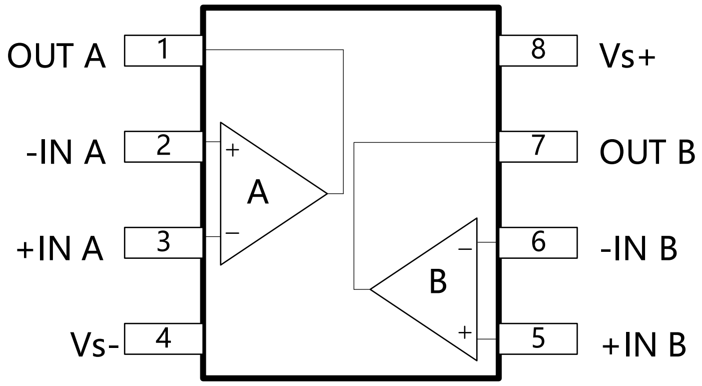
LTA6051
SOT23-5

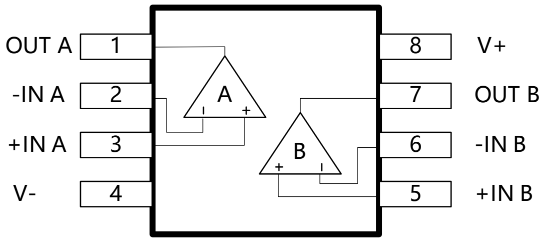


LTA6051
SOIC-8L

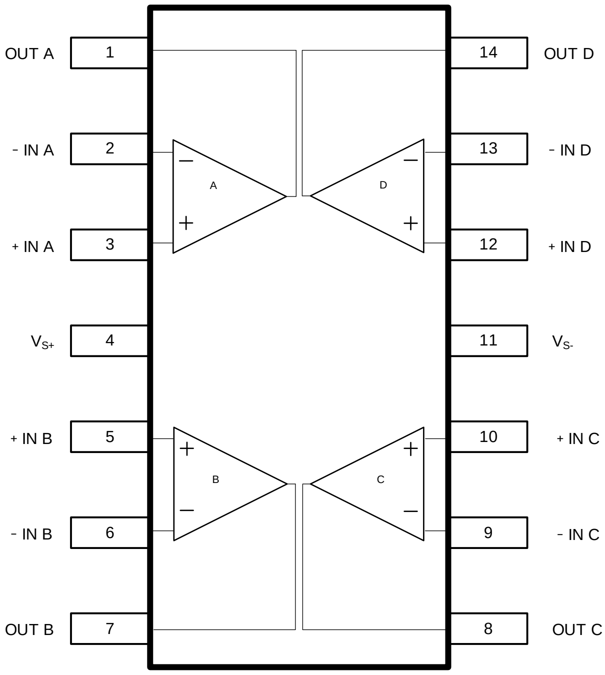


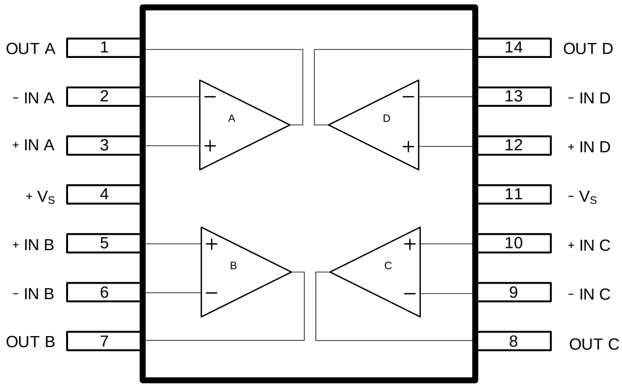
PIN Name	SOT23-5L	SOIC-8L	Description
OUT	1	6	Amplifier output.
V_{S-}	2	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.
+IN	3	3	Non-inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
-IN	4	2	Inverting input of the amplifier. This pin has the same voltage range as –IN.
V_{S+}	5	7	Positive power supply. The voltage is from 3.3 V to 12.6 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.
NC	-	1, 5, 8	No Connection





PIN Name	SOIC-8L / MSOP-8L	Description
OUT A	1	Amplifier A output.
-IN A	2	Inverting input A of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
+IN A	3	Non-inverting input of the amplifier. This pin has the same voltage range as –IN A.
V_{S-}	4	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.
+IN B	5	Non-inverting input of the amplifier. This pin has the same voltage range as –IN B.
-IN B	6	Inverting input B of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
OUT B	7	Amplifier B output.
V_{S+}	8	Positive power supply. The voltage is from 3.3 V to 12.6 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.





PIN Name	SOIC-14L / TSSOP-14L	Description
OUT A	1	Amplifier A output.
-IN A	2	Inverting input A of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
+IN A	3	Non-inverting input of the amplifier. This pin has the same voltage range as –IN A.
V_{s+}	4	Positive power supply. The voltage is from 3.3 V to 12.6 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.
+IN B	5	Non-inverting input of the amplifier. This pin has the same voltage range as –IN B.
-IN B	6	Inverting input B of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
OUT B	7	Amplifier B output.
OUT C	8	Amplifier C output.
-IN C	9	Inverting input C of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
+IN C	10	Non-inverting input of the amplifier. This pin has the same voltage range as –IN C.
V_{s-}	11	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 3.3 V to 12.6 V.
+IN D	12	Non-inverting input of the amplifier. This pin has the same voltage range as –IN D.
-IN D	13	Inverting input D of the amplifier. The voltage range is from (V_{S-} – 0.1 V) to (V_{S+} - 1 V).
OUT D	14	Amplifier D output.

Limiting Value

In accordance with the Absolute Maximum Ratin System (IEC60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	13.2 V
Signal Input Terminals: Voltage	V_{S-} – 0.5 V to V_{S+} + 0.5 V
Signal Input Terminals: Current	± 10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	−65 °C to +150 °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ESDA/JEDEC JS-001-2023 (1)	±8 000	V
Charged device model (CDM), per JESD22-A115C-2010	±1 000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Thermal Information

Thermal Metric		Package	Level	Unit
θ_{JA}	Package Thermal Resistance	SOT23-5L	190	°C/W
		SOIC-8L	125	
		MSOP-8L	216	
		TSSOP-14L	112	
		SOIC-14L	115	

10 V Electrical Characteristics

Unless otherwise noted, V_S = ±5.0 V, V_{cm} = 0V, A_V = +1, R_F = 20 Ω; $A_V \geq$ +2, R_F = 470 Ω and R_L = 100 Ω.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE						
-3dB Small-Signal Bandwidth	f_{-3dB}	G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 150 Ω		250		MHz
		G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 1 kΩ		300		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		90		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 1 kΩ		110		
Gain-Bandwidth Product	GBP	G= +10, R_L = 150 Ω		13		MHz
		G= +10, R_L = 1 kΩ		13.5		
Bandwidth for 0.1dB Flatness	$f_{0.1dB}$	G = +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		10.6		MHz
Slew Rate	SR	G = +1, V_{IN} = 2 V_{P-P}		180/190		V/µs
Rise Time	T_r	G = +1, V_{IN} = 0.2 V Step		2		ns
Fall Time	T_f	G = +1, V_{IN} = 0.2 V Step		1.5		ns
Settling Time to 0.1%	T_s	G= -1, R_F = 402 Ω, V_{OUT} = 2 V Step		14		ns
NOISE and DISTORTION PERFORMANCE						
Input Voltage Noise Density	e_n	f ≥ 1 MHz		1		nV/√Hz
DC PERFORMANCE						
Input Offset Voltage	V_{OS}			±2	±12	mV
Input Offset Voltage vs Temperature	dV_{os} / dT	T_A = -40°C to 125°C		4		µV/°C
Input Bias Current	I_B			3		pA
Input Offset Current	I_{OS}			0.5		pA
Open-loop voltage gain	A_{VOL}	R_L = 100 Ω, V_O = 4V_{p-p}		80	100	dB
INPUT CHARACTERISTICS						
Input Common Mode Voltage Range	V_{CM}		V_{S-} - 0.1		V_{S+} -1	V
Common Mode Rejection Rate	CMRR	G = +100, V_{CM} = -4.7 V to +3.5 V	60	80	108	dB
OUTPUT CHARACTERISTICS						
High Output Voltage Swing	V_{OH}	No Load	V_{S+} - 95	V_{S+} - 50		mV
		R_L = 100 Ω	V_{S+} - 750	V_{S+} - 550		
Low Output Voltage Swing	V_{OL}	No Load		V_{S-} +10	V_{S-} +40	mV
		R_L = 100 Ω		V_{S-} +300	V_{S-} +450	
Short-circuit Current	I_{source}	Open loop, Vin = ± 200 mV, No load		190		mA
	I_{sink}			210		
POWER SUPPLY						
Operating Supply Voltage	Vs	T_A = -40 to +125 °C	3.3		12.6	V
Quiescent Current (Per amplifier)	I_Q			7.4	9	mA

5 V Electrical Characteristics

Unless otherwise noted, V_S = ±2.5 V, V_{cm} = 0V, A_V = +1, R_F = 20 Ω; $A_V \geq +2$, R_F = 470 Ω and R_L = 100 Ω.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE						
-3dB Small-Signal Bandwidth	f_{-3dB}	G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 150 Ω		200		MHz
		G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 1 kΩ		240		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		85		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 1 kΩ		110		
Gain-Bandwidth Product	GBP	G= +10, R_L = 150 Ω		12		MHz
		G= +10, R_L = 1 kΩ		12.5		
Bandwidth for 0.1dB Flatness	$f_{0.1dB}$	G = +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		8		MHz
Slew Rate	SR	G = +1, V_{IN} = 2 V_{P-P}		160/180		V/µs
Rise Time	T_r	G = +1, V_{IN} = 0.2 V Step		2.2		ns
Fall Time	T_f	G = +1, V_{IN} = 0.2 V Step		1.8		ns
Settling Time to 0.1%	T_s	G= -1, R_F = 402 Ω, V_{OUT} = 2 V Step		13.5		ns
NOISE and DISTORTION PERFORMANCE						
Input Voltage Noise Density	e_n	f ≥ 1 MHz		1		nV/√Hz
Differential Gain	DG	G = +2, R_L = 150 Ω		0.05		%
Differential Phase	DP	G = +2, R_L = 150 Ω		0.05		°
DC PERFORMANCE						
Input Offset Voltage	V_{OS}			±1.8	±12	mV
Input Offset Voltage vs Temperature	dV_{os} / dT	T_A = -40°C to 125°C		4		µV/°C
Input Bias Current	I_B			0.5		pA
Input Offset Current	I_{OS}			0.2		pA
Open-loop voltage gain	A_{VOL}	R_L = 100 Ω, V_O = 3.3 V_{p-p}		80	100	dB
INPUT CHARACTERISTICS						
Input Common Mode Voltage Range	V_{CM}		V_{S-} - 0.1		V_{S+} -1	V
Common Mode Rejection Rate	CMRR	G = +100, V_{CM} = -2.2 V to +1 V	60	80	108	dB
OUTPUT CHARACTERISTICS						
High Output Voltage Swing	V_{OH}	No Load	V_{S+} - 80	V_{S+} - 40		mV
		R_L = 100 Ω	V_{S+} - 450	V_{S+} - 350		
Low Output Voltage Swing	V_{OL}	No Load		V_{S-} +5	V_{S-} +20	mV
		R_L = 100 Ω		V_{S-} +100	V_{S-} +250	
Short-circuit Current	I_{source}	Open loop, Vin = ± 200 mV, No load		120		mA
	I_{sink}			140		
POWER SUPPLY						
Operating Supply Voltage	Vs	T_A = -40 to +125 °C	3.3		12.6	V
Quiescent Current (Per amplifier)	I_Q			6.7	8	mA

3.3 V Electrical Characteristics

Unless otherwise noted, V_S = ±1.65 V, V_{cm} = 0V, A_V = +1, R_F = 20 Ω; $A_V \geq$ +2, R_F = 470 Ω and R_L = 100 Ω.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE						
-3dB Small-Signal Bandwidth	f_{-3dB}	G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 150 Ω		160		MHz
		G= +1, V_{OUT} = 0.2 V_{P-P}, R_F =20 Ω, R_L = 1 kΩ		200		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		80		
		G= +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 1 kΩ		105		
Gain-Bandwidth Product	GBP	G= +10, R_L = 150 Ω		12		MHz
		G= +10, R_L = 1 kΩ		12.5		
Bandwidth for 0.1dB Flatness	$f_{0.1dB}$	G = +2, V_{OUT} = 0.2 V_{P-P}, R_F =470 Ω, R_L = 150 Ω		7		MHz
Slew Rate	SR	G = +1, V_{IN} = 2 V_{P-P}		150/170		V/µs
Rise Time	T_r	G = +1, V_{IN} = 0.2 V Step		4		ns
Fall Time	T_f	G = +1, V_{IN} = 0.2 V Step		4		ns
Settling Time to 0.1%	T_s	G= -1, R_F = 402 Ω, V_{OUT} = 2 V Step		16.5		ns
NOISE and DISTORTION PERFORMANCE						
Input Voltage Noise Density	e_n	f ≥ 1 MHz		1		nV/√Hz
DC PERFORMANCE						
Input Offset Voltage	V_{OS}			±1.5	±12	mV
Input Offset Voltage vs Temperature	dV_{os} / dT	T_A = -40°C to 125°C		3		µV/°C
Input Bias Current	I_B			0.6		pA
Input Offset Current	I_{OS}			0.6		pA
Open-loop voltage gain	A_{VOL}	R_L = 100 Ω, V_O = 1.8 V_{p-p}		70	80	dB
INPUT CHARACTERISTICS						
Input Common Mode Voltage Range	V_{CM}		V_{S-} - 0.1		V_{S+} -1	V
Common Mode Rejection Rate	CMRR	G = +100, V_{CM} = -1.65 V to +0.35 V	55	60	90	dB
OUTPUT CHARACTERISTICS						
High Output Voltage Swing	V_{OH}	No Load	V_{S+} - 50	V_{S+} - 30		mV
		R_L = 100 Ω	V_{S+} - 350	V_{S+} - 300		
Low Output Voltage Swing	V_{OL}	No Load		V_{S-} +3	V_{S-} +5	mV
		R_L = 100 Ω		V_{S-} +180	V_{S-} +200	
Short-circuit Current	I_{source}	Open loop, Vin = ± 200 mV, No load		70		mA
	I_{sink}			90		
POWER SUPPLY						
Operating Supply Voltage	Vs	T_A = -40 to +125 °C	3.3		12.6	V
Quiescent Current (Per amplifier)	I_Q			6.3	7	mA

Typical Characteristics

At T_A = 25℃, V_S = ±5 V, R_F = 20 Ω for G = +1, R_F = 470 Ω for G = +2, G= +10, and R_L = 150 Ω, unless otherwise noted.

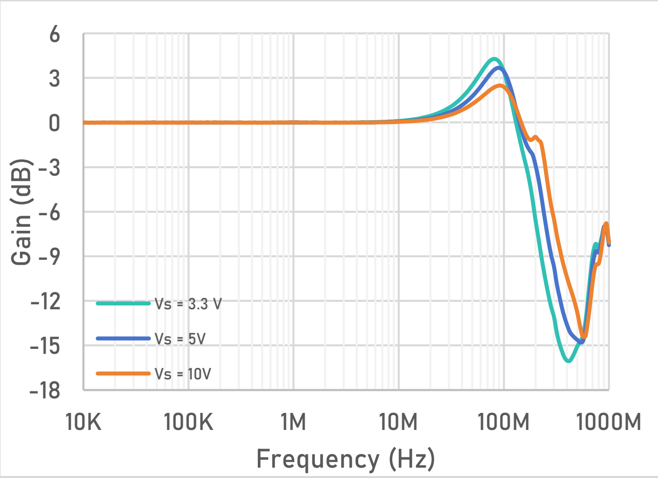


Figure 1. Closed-loop Bandwidth (G = +1)

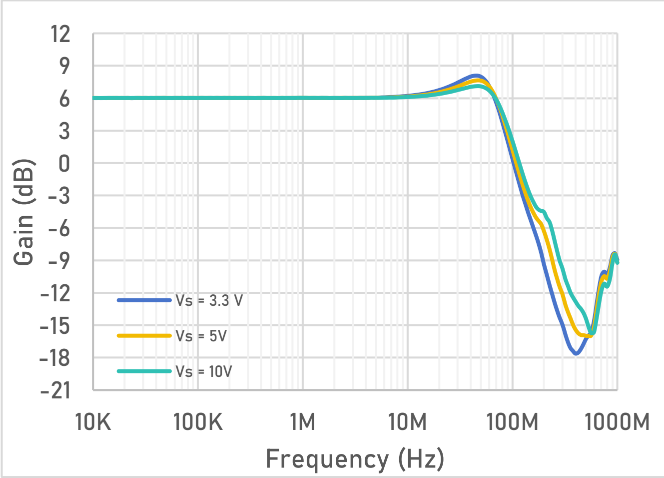


Figure 2. Closed-loop Bandwidth (G = +2)

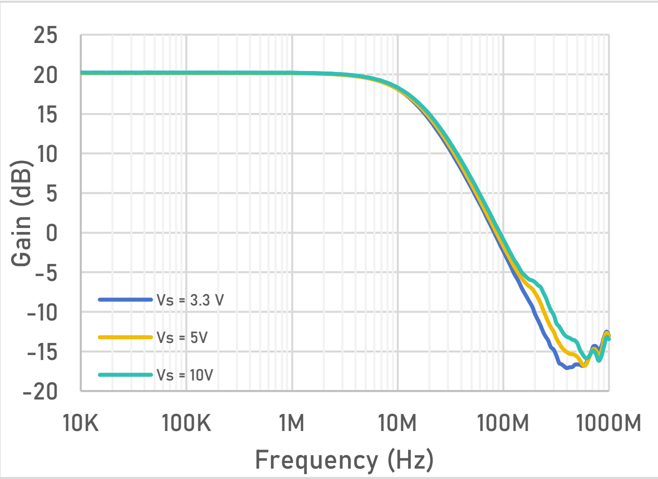


Figure 3. Closed-loop Bandwidth (G = + 10)

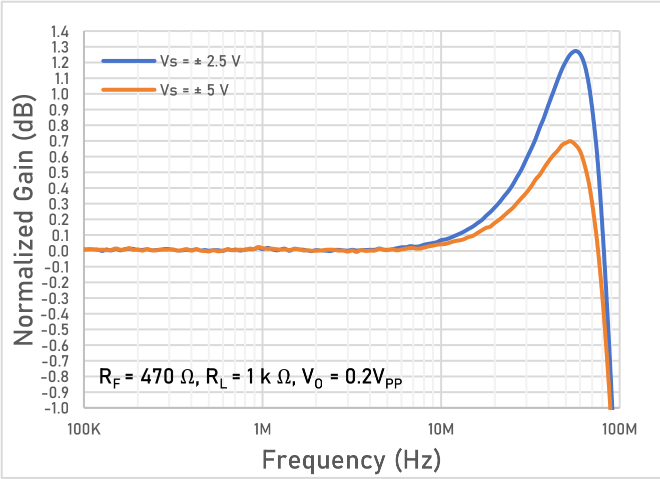


Figure 4. 0.1 dB Gain Flatness (G= +2)

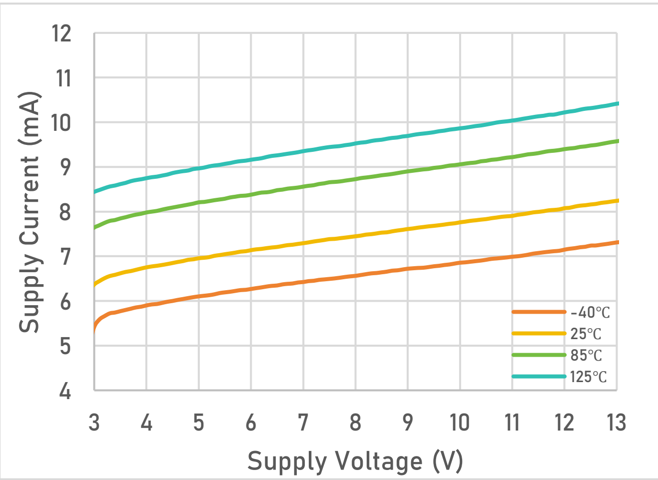


Figure 5. Supply Current per Channel vs Supply Voltage

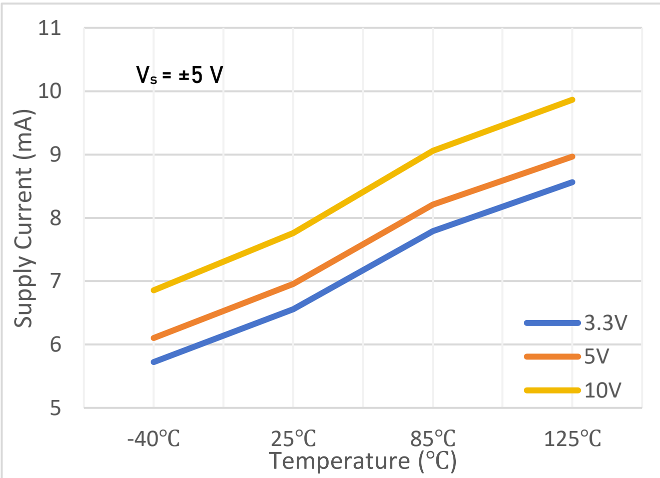


Figure 6. Supply Current per Channel vs Temperature

Typical Characteristics (Cont.)

At T_A = 25℃, V_S = ±5 V, R_F = 20 Ω for G = +1, R_F = 470 Ω for G = +2, G= +10, and R_L = 150 Ω, unless otherwise noted.

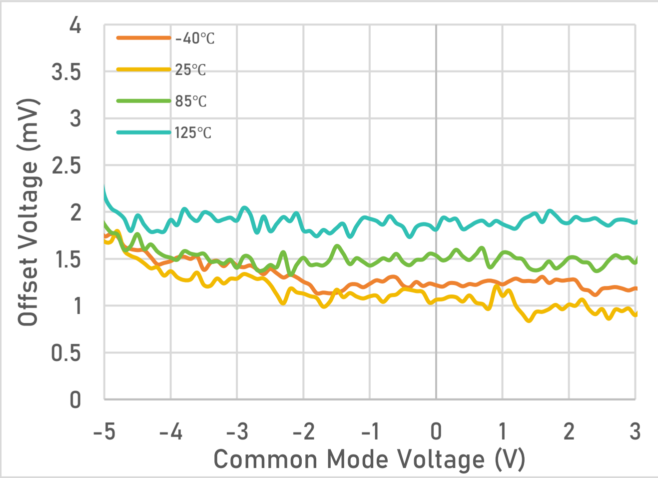


Figure 7. Offset Voltage vs Common Mode Voltage (V_s = ± 5V)

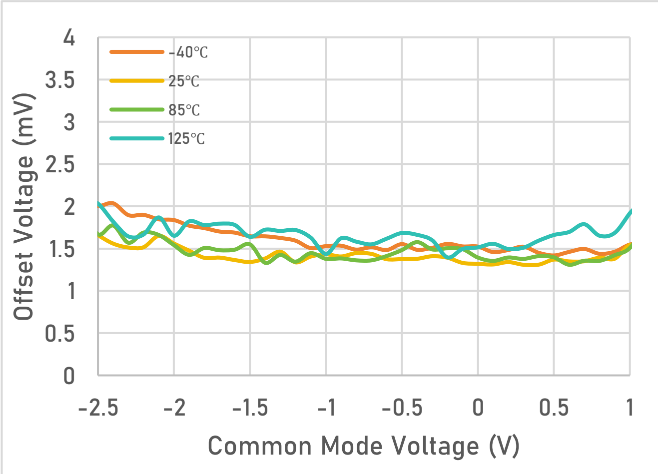


Figure 8. Offset Voltage vs Common Mode Voltage (V_s = ± 2.5 V)

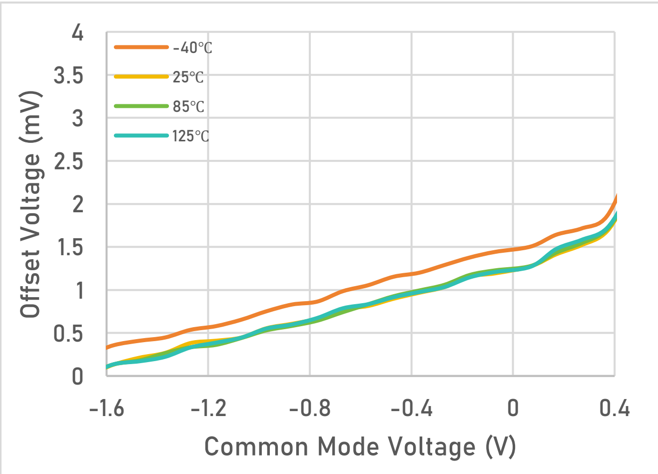


Figure 9. Offset Voltage vs Common Mode Voltage (V_s = ± 1.65 V)

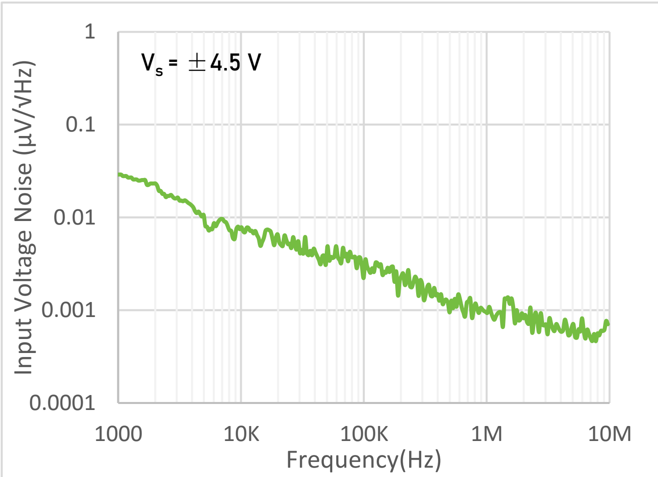


Figure 10. Input Voltage Noise vs Frequency

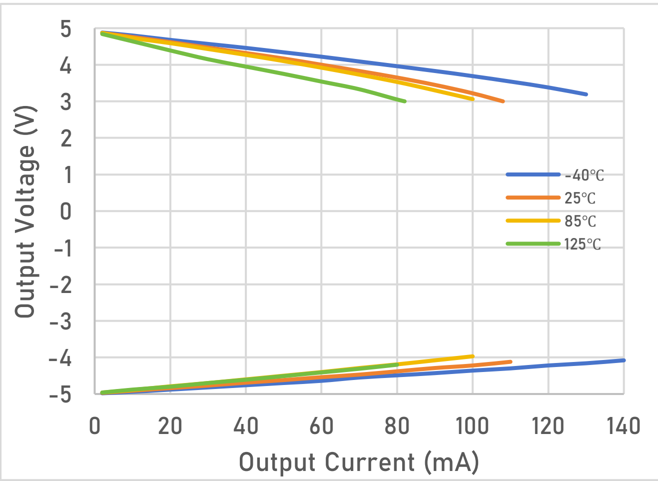


Figure 11. Output Voltage vs Output Current (V_s = ± 5 V)

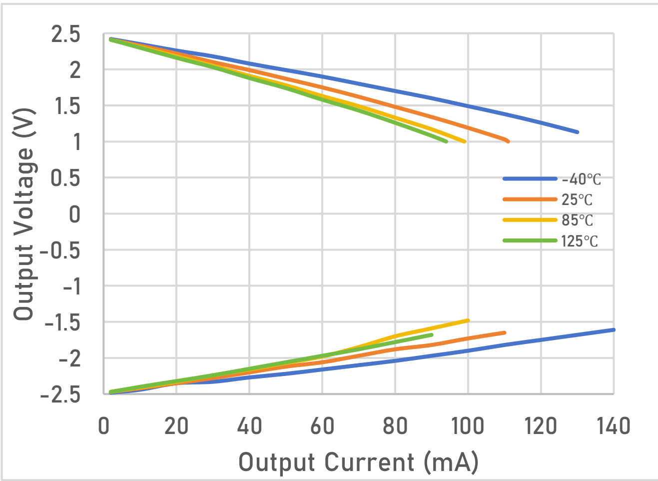


Figure 12. Output Voltage vs Output Current (V_s = ± 2.5 V)

Typical Characteristics (Cont.)

At T_A = 25℃, V_S = ±5 V, R_F = 20 Ω for G = +1, R_F = 470 Ω for G = +2, G= +10, and R_L = 150 Ω, unless otherwise noted.

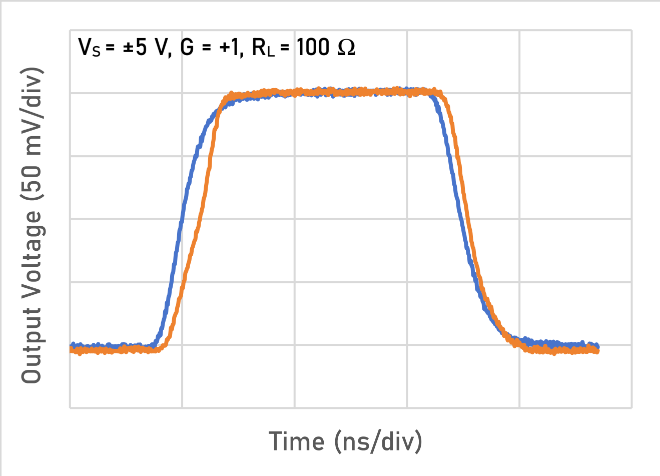


Figure 13. Non-Inverting Small-Signal Step Response

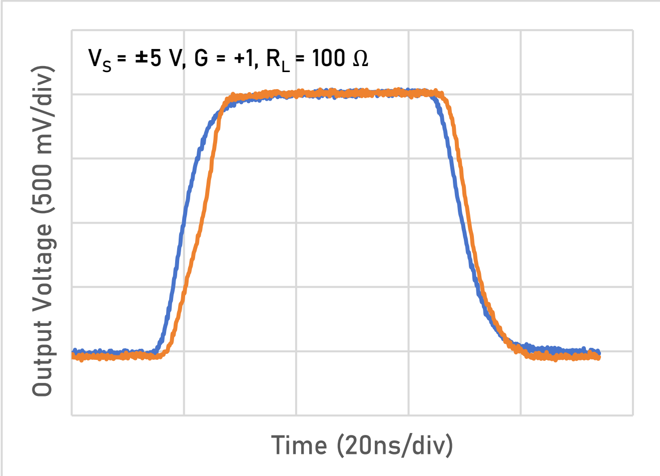


Figure 14. Non-Inverting Large-Signal Step Response

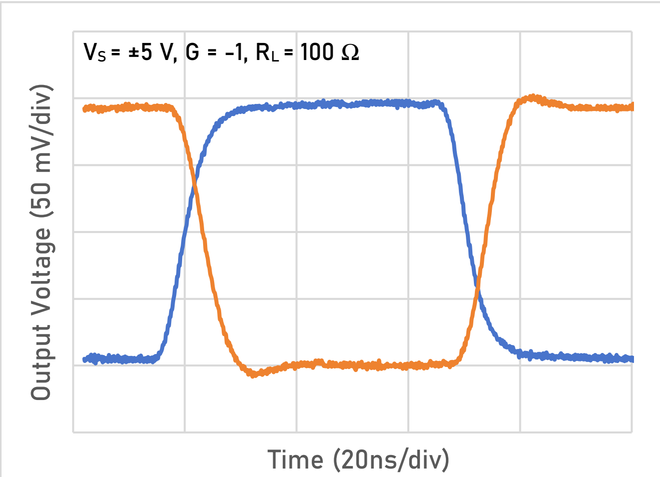


Figure 15. Inverting Small-Signal Step Response

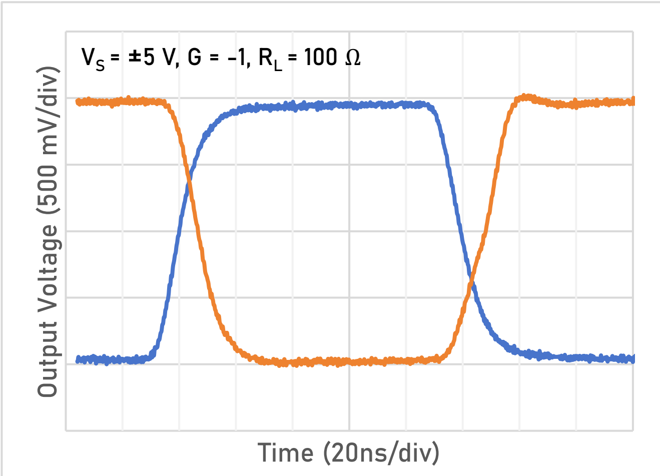


Figure 16. Inverting Large-Signal Step Response

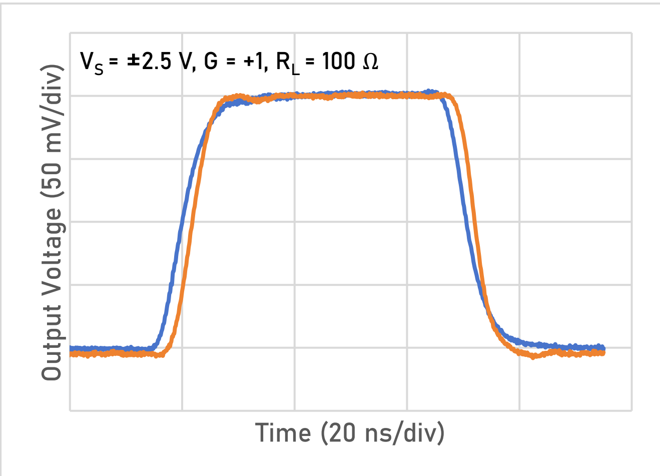


Figure 17. Non-Inverting Small-Signal Step Response

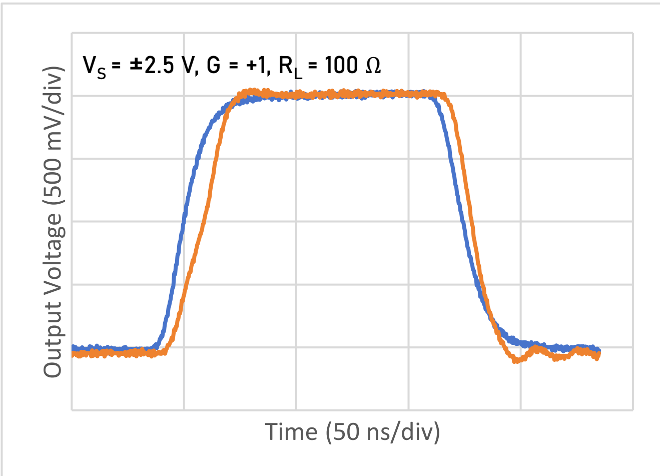


Figure 18. Non-Inverting Large-Signal Step Response

Typical Characteristics (Cont.)

At T_A = 25℃, V_S = ±5 V, R_F = 20 Ω for G = +1, R_F = 470 Ω for G = +2, G= +10, and R_L = 150 Ω, unless otherwise noted.

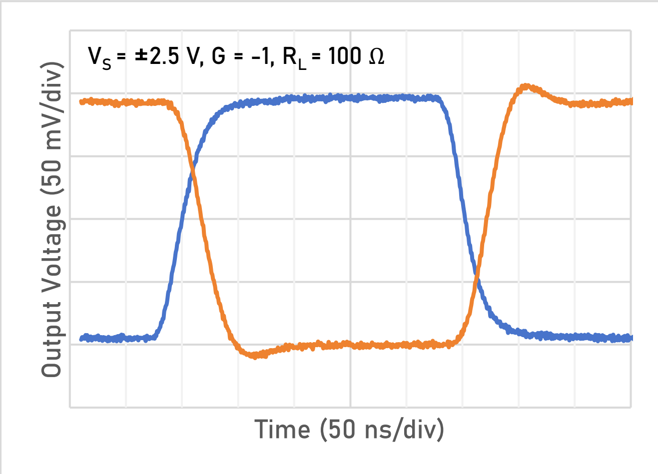


Figure 19. Inverting Small-Signal Step Response

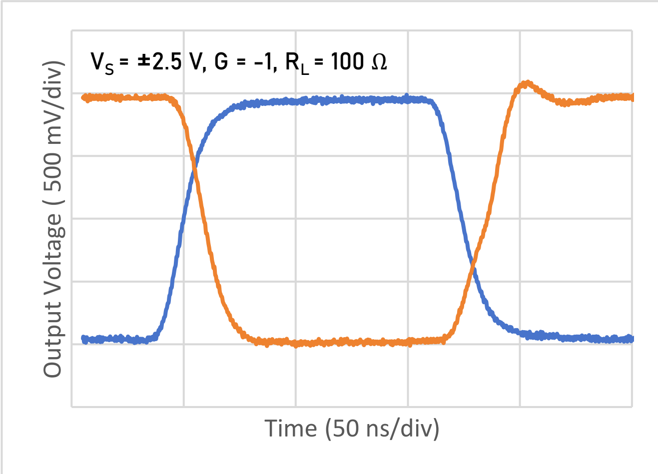


Figure 20. Inverting Large-Signal Step Response

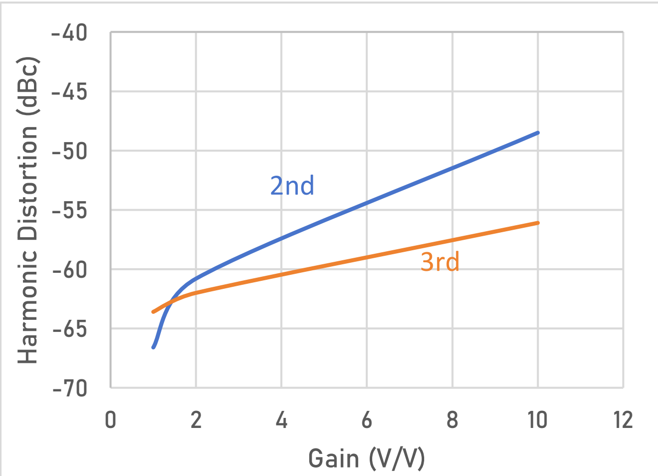


Figure 21. Harmonic Distortion vs Gain
Vs=±2.5V, f = 1MHz, V_o = $2V_{pp}$

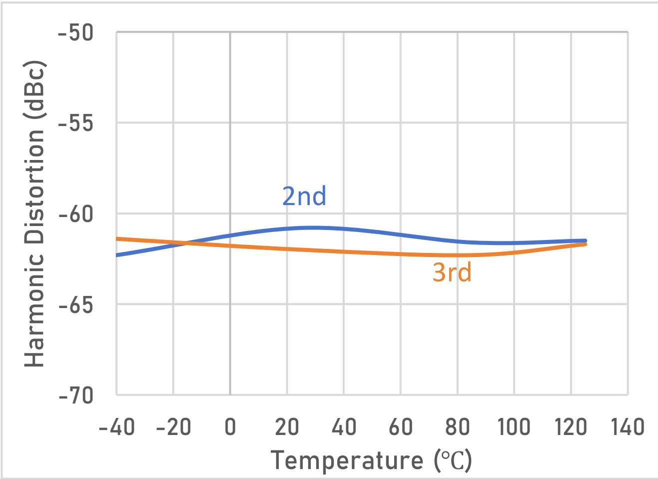


Figure 22. Harmonic Distortion vs Temperature
Vs=±2.5V, f = 1MHz, V_o = $2V_{pp}$

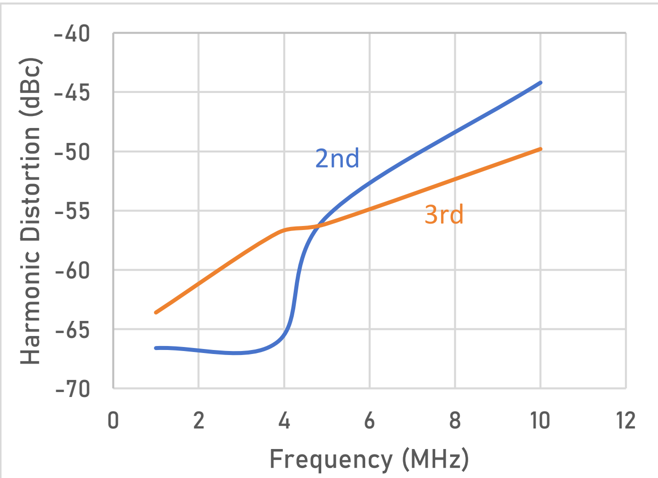


Figure 23. Harmonic Distortion vs Frequency
Vs=±2.5V, G = +1, V_o = $2V_{pp}$

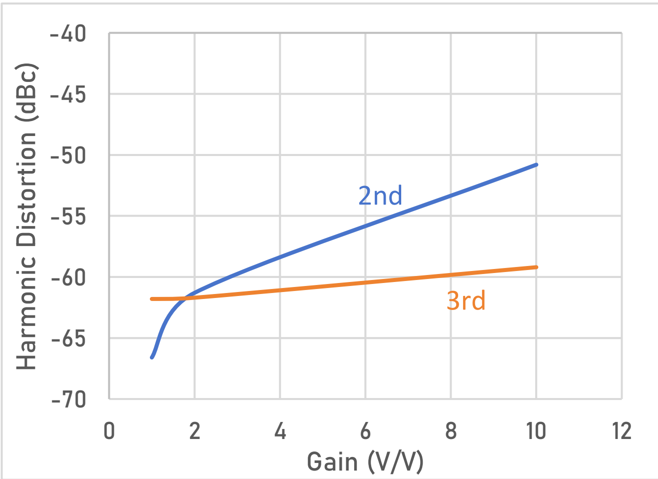


Figure 24. Harmonic Distortion vs Gain
Vs=±5V, f = 1MHz, V_o = $2V_{pp}$

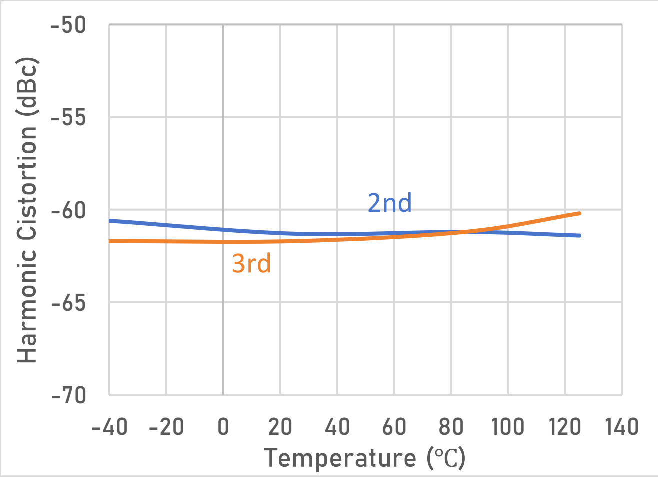


Figure 25. Harmonic Distortion vs Temperature
Vs=±5V, f = 1MHz, V_o = $2V_{pp}$

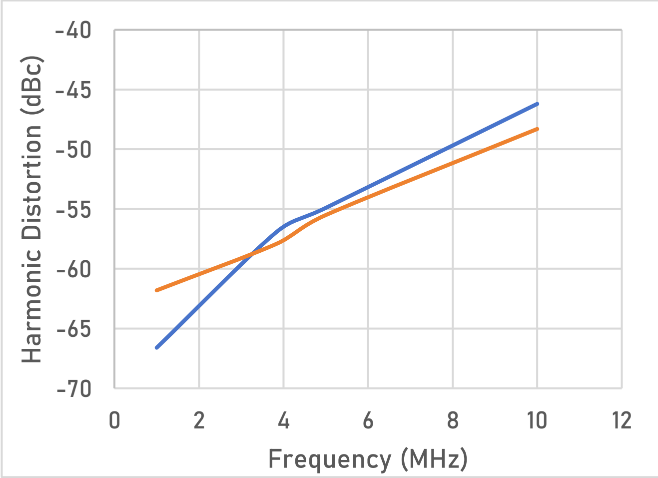


Figure 26. Harmonic Distortion vs Temperature
Vs=±5V, G = +1, V_o = $2V_{pp}$

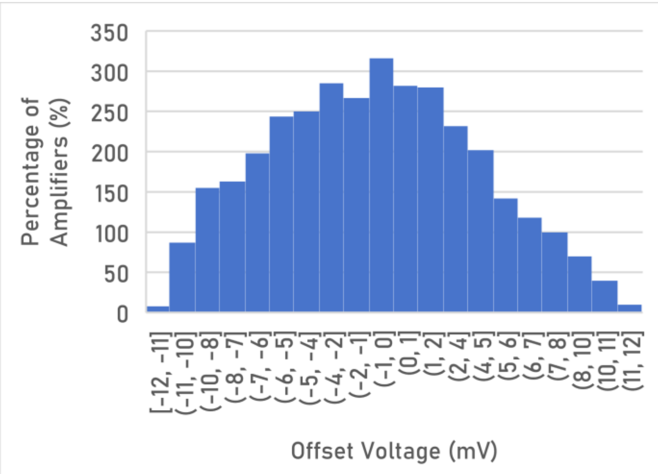


Figure 27. Offset Voltage Production Distribution

Detailed Description

The LTA605x is a family of High speed, high slew rate, rail-to-rail output operational amplifiers specifically designed for high-speed applications. These devices operate from 3.3 V to 12.6 V at the temperature range of −40 ℃ to +125 ℃, are unity-gain stable, and suitable for a wide range of general-purpose applications. The output stage is capable of driving heavy loads with 130 mA linear output current. The input common-mode voltage range includes from V_{S-} -0.1 V to V_{S+} -1 V, and allows the LTA605x family to be used in virtually any single supply application. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The LTA605x features 250 MHz bandwidth and 190 V/μs slew rate, providing good ac performance at same time. DC applications are also well served with low input bias current, and an input offset voltage of ±2 mV typically. The typical offset voltage drift is 4 μV/℃, over the full temperature range the input offset voltage changes only 660 μV.

Operating Voltage

The LTA605x family is optimized for operation at voltages as low as +3.3 V (±1.65 V) and up to +12.6 V (±6.3 V). In addition, many specifications apply from −40 ℃ to +125 ℃. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

Rail to rail output

Designed as a high speed, high slew rate, low-noise operational amplifier, the LTA605x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100 Ω, the output swings typically to within 750-mV of 10 V supply rail. Different load conditions change the ability of the amplifier to swing close to the rails. For in open load, the output swings typically to within 95 mV of the positive supply rail and within 40 mV of the negative supply rail.

Capacitive load and stability

As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTA605x op-amps must drive a heavy capacitive load. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 1. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

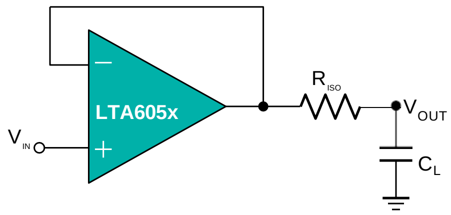


Figure 1. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

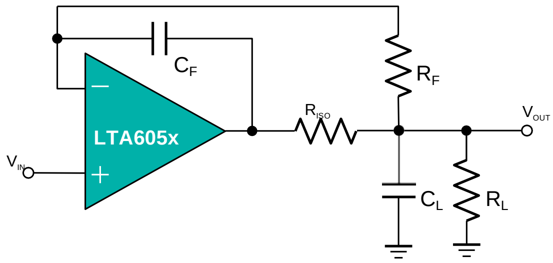


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

Typical Application Circuit

Active filter

The LTA605x family is well-suited for active filter applications that require a wide bandwidth, fast slew rate, single-supply operational amplifier. Figure 3 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cut-off frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

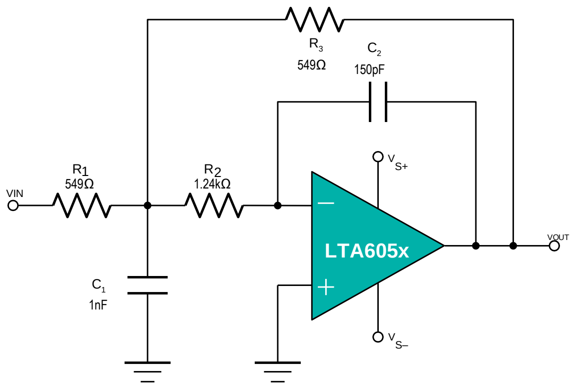


Figure 3. Second-Order, Butterworth, 500-kHz Low- Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a non- inverting output can be achieved through one of these options:

1. adding an inverting amplifier ;
2. adding an additional second-order MFB stage;
3. using a non-inverting filter topology, such as the Sallen-Key (shown in Figure 4).

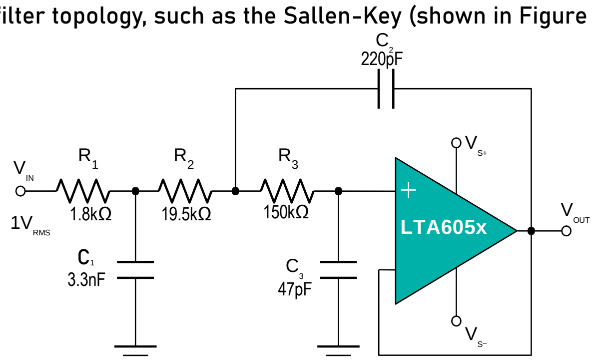


Figure 4. Configured as a Three-Pole, 20-kHz, Sallen- Key Filter

Differential amplifier

The circuit shown in Figure 5 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}$

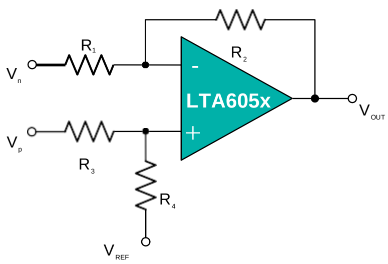
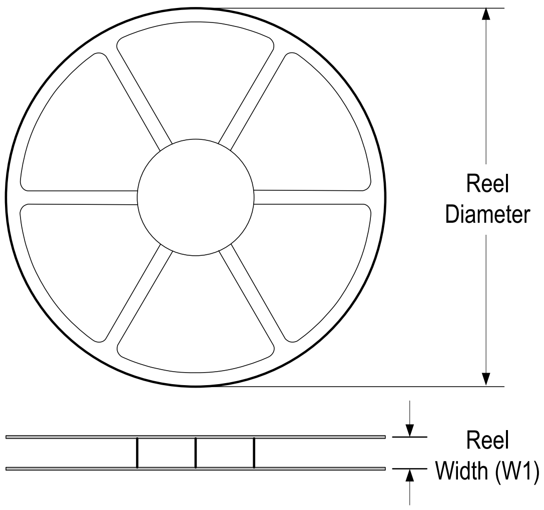


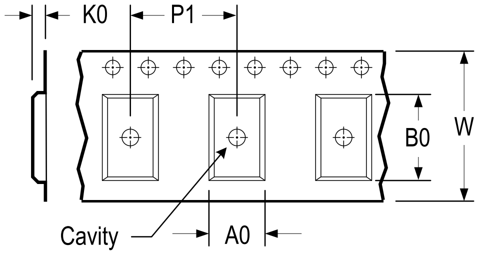
Figure 5. Differential Amplifier

Tape and Reel Information

REEL DIMENSIONS

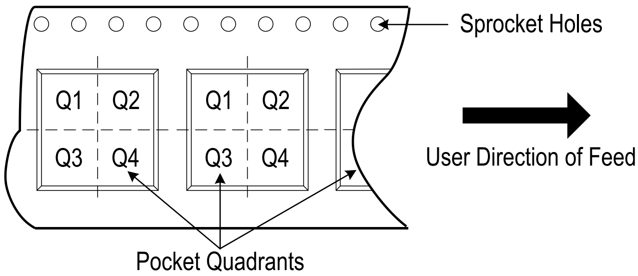


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

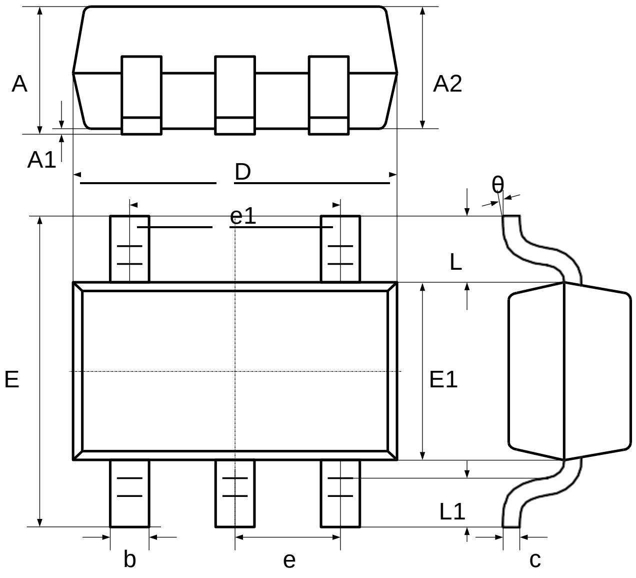


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA6051XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA6051XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6052XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6052XV8/R6	MSOP	8	3 000	330	12.4	5.0	3.5	2.0	8.0	12.0	Q1
LTA6054XS14/R5	SOIC	14	2 500	330	12.4	6.5	9.5	2.0	8.0	16.0	Q1
LTA6054XT14/R6	TSSOP	14	3 000	330	12.4	6.9	5.5	1.2	8.0	16.0	Q1

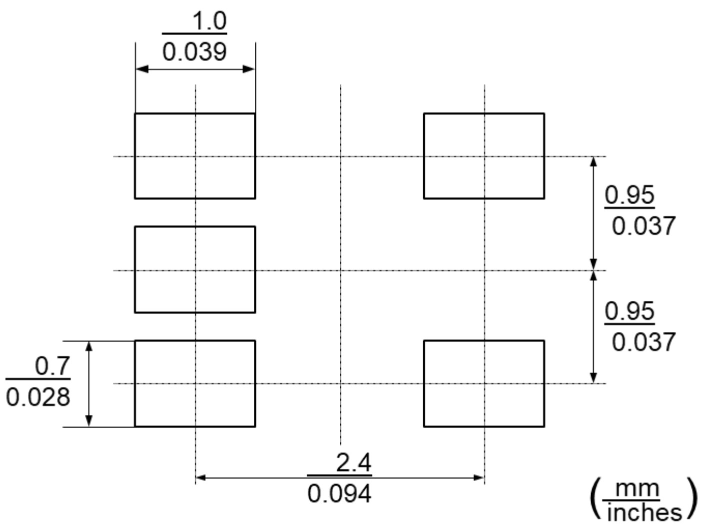
Package Outlines

DIMENSIONS, SOT23-5L



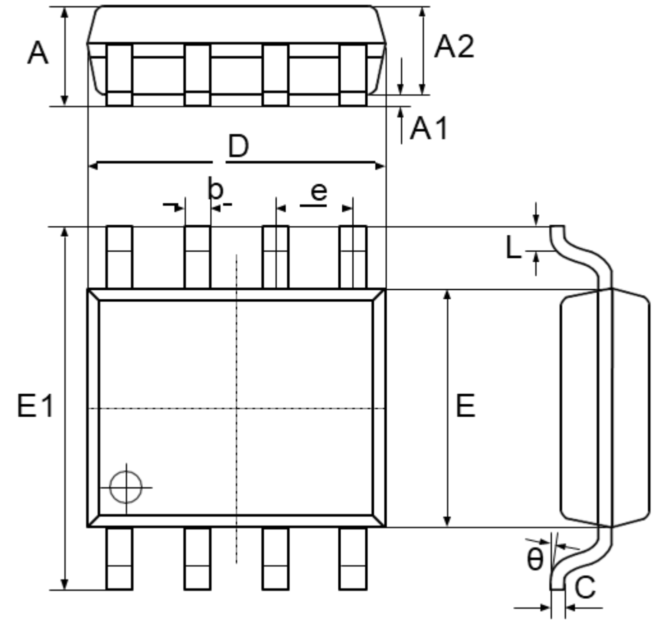
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



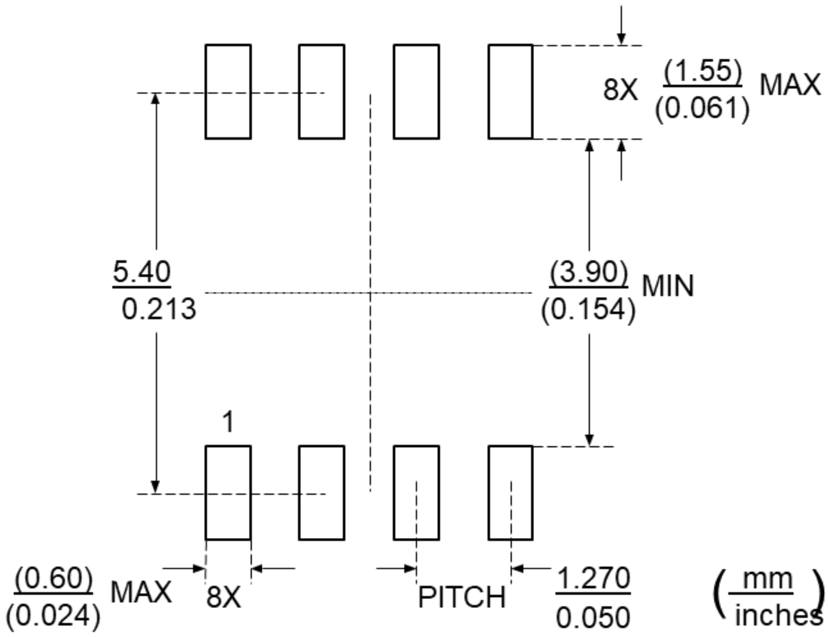
Package Outlines (cont.)

DIMENSIONS, SOIC-8L



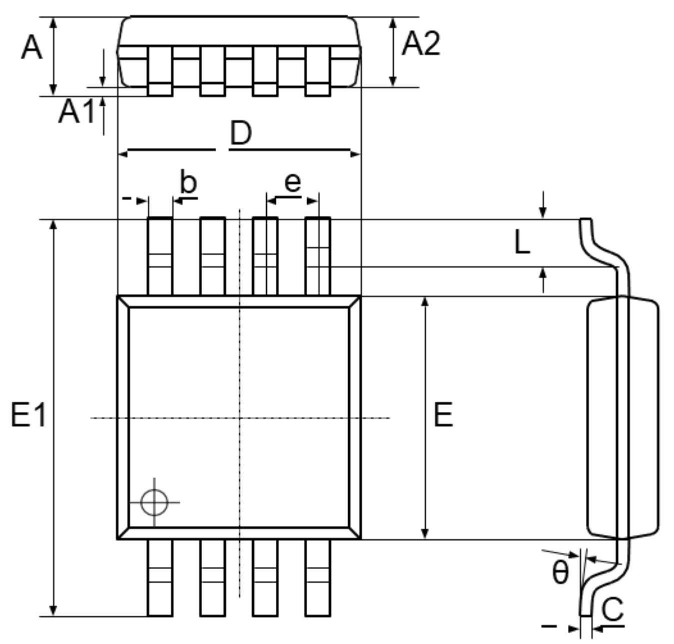
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



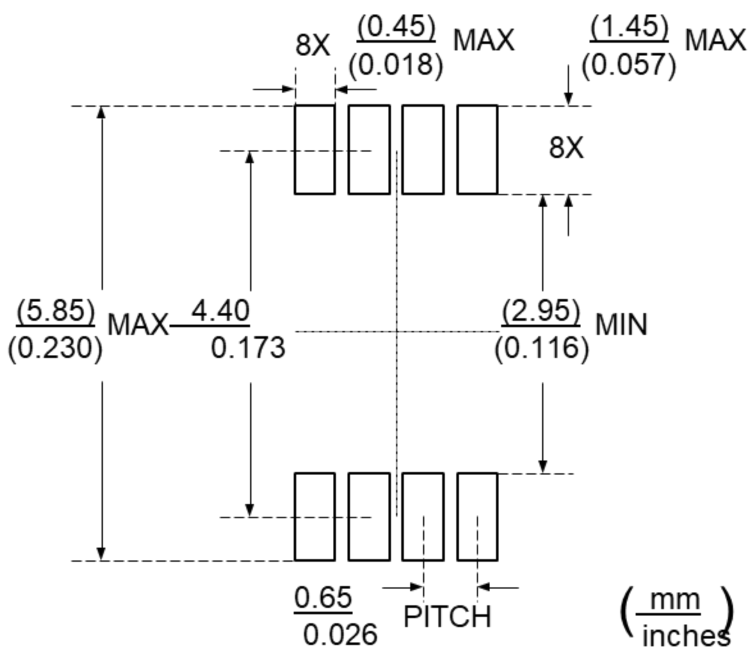
Package Outlines (cont.)

DIMENSIONS, MSOP-8L



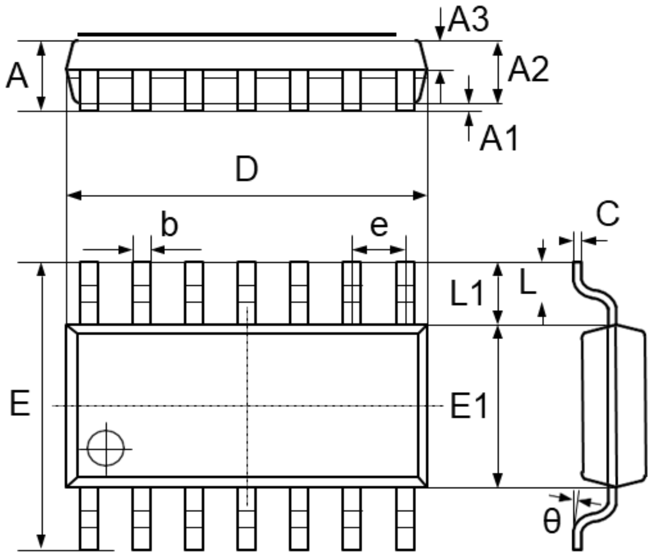
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



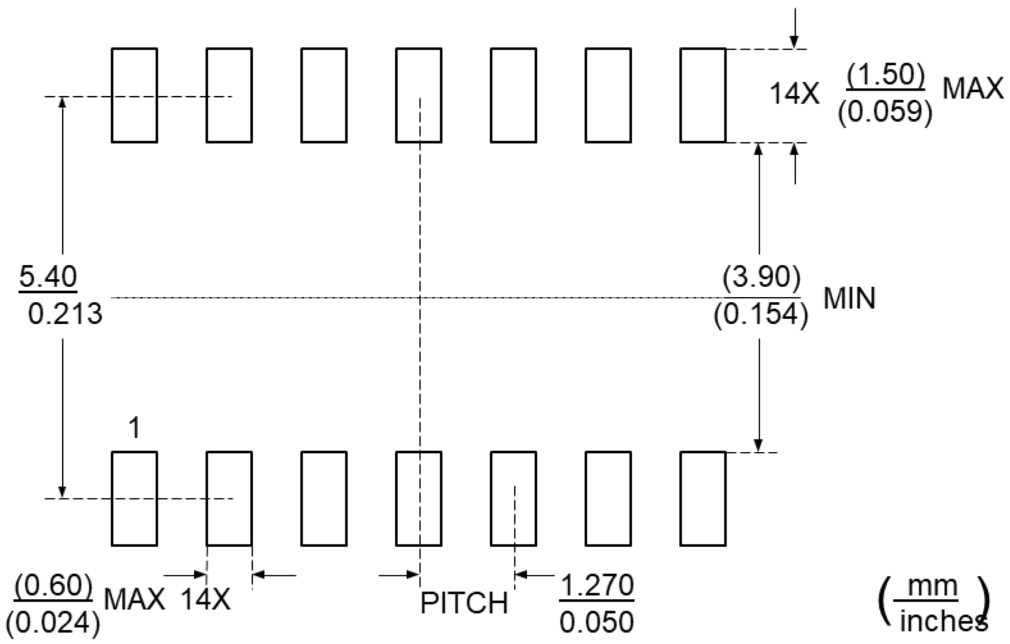
Package Outlines (Cont.)

DIMENSIONS, SOIC-14L



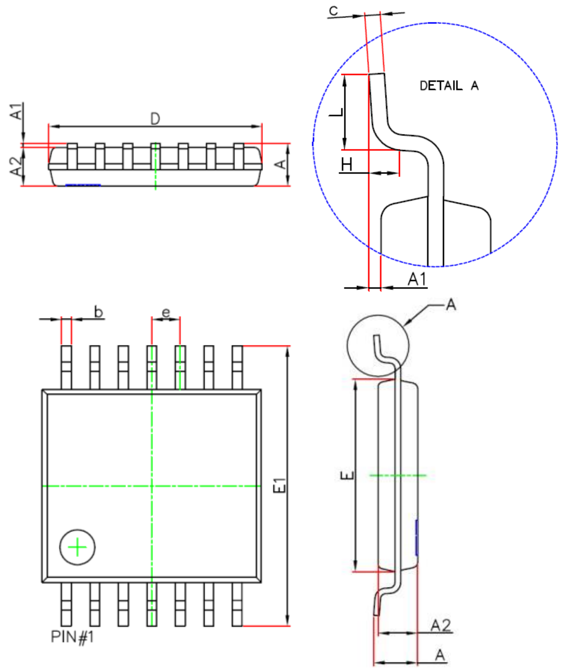
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.057	0.073
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
A3	0.550	0.750	0.022	0.030
b	0.406 TYP.		0.016 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.340	0.348
E	5.840	6.240	0.230	0.246
E1	3.850	4.050	0.152	0.159
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.030
θ	2°	8°	2°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



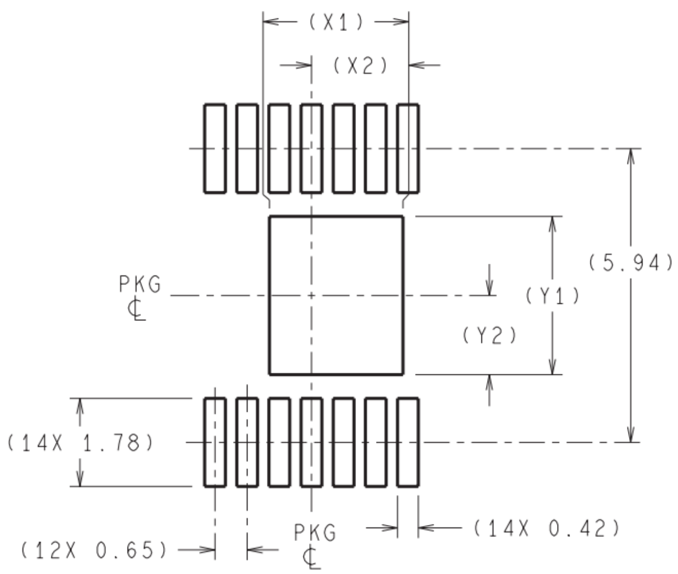
Package Outlines (Cont.)

DIMENSIONS, TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.9	5.1	0.193	0.201
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A	—	1.2	—	0.047
A2	0.8	1	0.031	0.039
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



Important Notice

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