LTA6771 LTA6772 LTA6773

4 ns, High Speed Comparator With Push-pull Outputs

General Description

The LTA6771/LTA6772/LTA6773 are single-, dual-, quad- channel comparators with push-pull output that feature 4ns propagation delay, a wide range of supply voltages from 2.7V to 5.5V with rail-to-rail inputs helps to implement in a wide variety of applications where require critical response time, power-sensitive, low-voltage. The output of the LTA6771/6772/6773 pulls to within 0.1 V of either supply rail without external pull-up circuitry, making it ideal for interface with CMOS or TTL logic directly. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The LTA6771 (single) is available in both SOT23-6L and SOIC-8L packages. The LTA6772 (dual) is offered in SOT23-8L, SOIC-8L and MSOP-8L packages, The LTA6773 (single) is offered in SOT23-5L and SC70-5L packages. All devices are rated over -40℃ to +125℃ extended industrial temperature range.

Features and Benefits

- Fast 4ns Propagation Delay (100-mV Overdrive)
- Rail-to-Rail I/O
- Shutdown version (LTA6771)
- Supply voltage : 2.7 V to 5.5 V
- Replacement for TLV3501, TLV3502
- Small packages: available in SOT23-5L,SC70-5L,SOT23-6L,SOIC-8L,SOT23-8L,MSOP-8L
- Low supply current : 3mA

Applications

- High speed instrumentation
- Clock and data signal restoration
- Pulse spectroscopy
- High speed line receivers
- Threshold detection
- Peak and zero-crossing detectors
- High speed trigger circuitry
- Pulse-width modulators
- Current/voltage-controlled oscillators
- Automatic test equipment (ATE)
- Wireless Base Stations

Table of Content

Revision History

Version FN1623-47.0

- Initial version.

Change from Revision FN1623-47.0 (Dec, 2023) to FN1623-47.1 (Jan, 2024)

- Change Propagation Delay Rising / Falling Edge graphs (Figure 6, Figure 7), Remove Figure 8, Figure 9

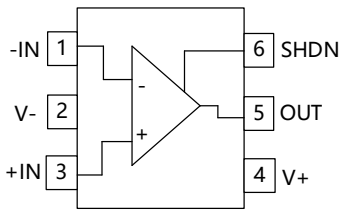
Ordering Information

Part Number	Package Type	Quantity	Mark Code
LTA6771XT6/R6*	SOT23-6L	Tape and Reel, 3000	R71
LTA6771XS8/R8*	SOIC-8L	Tape and Reel, 4000	R6771
LTA6772XT8S/R6	SOT23-8L	Tape and Reel, 3000	R6772
LTA6772XS8/R8	SOIC-8L	Tape and Reel, 4000	R6772
LTA6772XV8/R6	MSOP-8L	Tape and Reel, 3000	R6772
LTA6773XT5/R6*	SOT23-5L	Tape and Reel, 3000	73U
LTA6773XC5/R6*	SC70-5L	Tape and Reel, 3000	73U

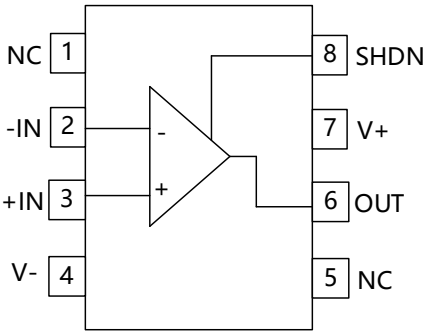
* Preview Status (Not for MP stage, pls contact with us if you have request)

Pin Configuration (Top View)

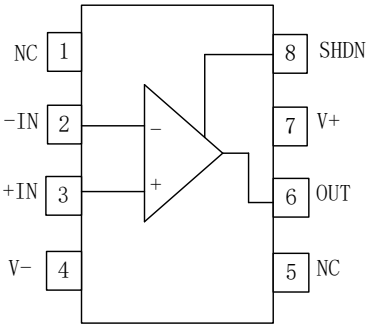
LTA6771
SOT23-6



LTA6771
SOIC-8L



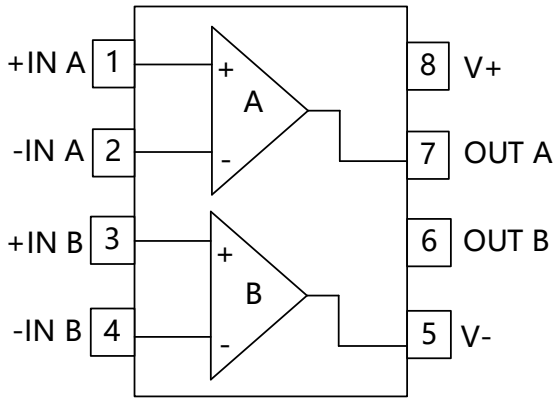
LTA6771
SOT23-8L



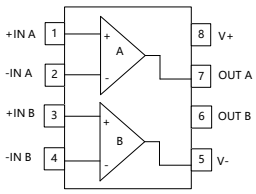
Pin Functions: LTA6771

Symbol	Pin Number		Description
	SOIC-8L/ SOT23-8L	SOT23-6L	
-IN	2	1	Negative (inverting) input
+IN	3	3	Positive (noninverting) input
NC	1,5	-	No internal connection (can be left floating)
OUT	6	5	Output
SHDN	8	6	Shutdown (the device is idle when this pin is not in use)
V-	4	2	Negative (lowest) power supply
V+	7	4	Positive (highest) power supply

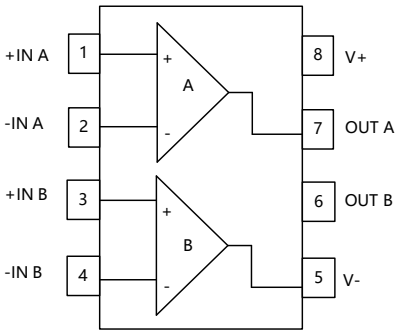
LTA6772
SOIC-8L



LTA6772
MSOP-8L



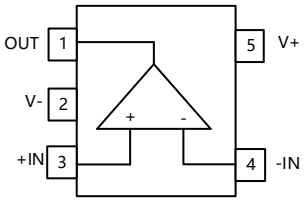
LTA6772
SOT23-8L



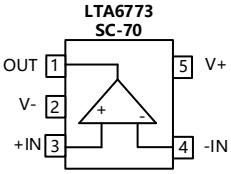
Pin Functions: LTA6772

Symbol	Pin Number SOIC-8L/MSOP8/SOT23-8	Description
-IN A	2	Inverting input, channel A
+IN A	1	Noninverting input, channel A
-IN B	4	Inverting input, channel B
+IN B	3	Noninverting input, channel B
OUT A	7	Output, channel A
OUT B	6	Output, channel B
V-	5	Nagative (lowest) power supply
V+	8	Positive (highest) power supply

LTA6773
SOT23-5



LTA6773
SC-70



Symbol	Pin Number SC70-5L/ SOT23-5L	Description
-IN	4	Negative (inverting) input
+IN	3	Positive (noninverting) input
OUT	1	Output
V-	2	Negative (lowest) power supply
V+	5	Positive (highest) power supply

Device comparison table

Device	V_{DD}	tPD+	tPD-	V_{HYST}	V_{os-max}	Output
LTA6771/2/3	1.8 V to 5.5 V	4 ns	4 ns	10 mV	3.5 mV	Push-pull
LTC8721/2/3	1.7 V to 5.5 V	78 ns	66 ns	3 mV	3.5 mV	Push-pull
LTC8741/2/3/4	1.8 V to 5.5 V	39 ns	33 ns	3 mV	3.5 mV	Push-pull

Limiting Value

PARAMETER		MIN	MAX	UNIT
Voltage	Supply		6.5	V
	Signal input terminal	(V-)-0.3	(V+) + 0.3	V
Current	Signal input terminal	TBD	TBD	mA
	Output short circuit	TBD	TBD	mA
Temperature	Operating, T_A	-40	125	℃
	Storage, T_{stg}	-65	150	℃

ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	TBD	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	TBD	V

Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_S	Supply voltage	2.7		5.5	V
V_{IL}	Low-level input voltage, SHDN (comparator is enabled)		TBD		V
V_{IH}	High-level input voltage,SHDN(comparator is disabled)		TBD		V
T_A	Operating temperature	-40		125	℃

Thermal Information

Thermal Metric		Package		Unit
θ_{JA}	Thermal Resistance	SOT23-6L	TBD	℃/W
		SOIC-8L	125	
		SOT23-8L	TBD	
		MSOP-8L	216	
		SOT23-5L	190	
		SC70-5L	333	

Electrical Characteristics

At T_A = 25°C and V_S = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM}=0 V, I_O=0 mA		2		mV
dV_{OS}/dT	Input offset voltage vs temperature	T_A = -40°C to +125°C		2		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V		500		µV/V
	Input hysteresis			10		mV
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V_{S-})-0.1		(V_{S+}) +0.1	V
CMRR	Common-mode rejection ratio	V_{CM}=-0.2V to (V+) +0.2V		60		dB
		V_{CM}=-0.2V to (V+) +0.2V, T_A=-40°C to +125°C		58		
OUTPUT						
V_{OH}, V_{OL}	Voltage output swing from rail	I_{OUT}=±1mA		20	50	mV
SHUTDOWN						
t_{OFF}	Shutdown turnoff time			TBD		ns
t_{ON}	Shutdown turnon time			TBD		ns
V_L	SHDN low threshold	Comparator is enabled		TBD		V
V_H	SHDN high threshold	Comparator is disabled		TBD		V
	Input bias current of shutdown pin			TBD		pA
I_{QSD}	Quiescent current in shutdown			TBD		µA
POWER SUPPLY						
V_S	Specified voltage		2.7		5.5	V
	Operating voltage range	Higher end		TBD		V
		Lower end		TBD		
I_Q	Quiescent current	V_S=5V, V_O=High		3	6	mA
TEMPERATURE RANGE						
	Operating range		-40		125	°C

At T_A = 25°C and V_S = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$T_{(pd)}$	Propagation delay time	V_{dd} = 5.5 V Input Overdrive = 20 mV	At T_A=25°C		6		ns
			At T_A=-40°C to 125°C		7		ns
		V_{dd} = 5.5 V Input Overdrive = 100 mV	At T_A=25°C		4		ns
			At T_A=-40°C to 125°C		5		ns
t_R	Rise time	Measured between 10% to 90% of Vs			1		ns
t_F	Fall time	Measured between 90% to 10% of Vs			1		ns

Typical Characteristics – LTA6772

T_J = +25 ℃, V_{DD} = 5.5 V and input overdrive = ±15 mV, unless otherwise noted.

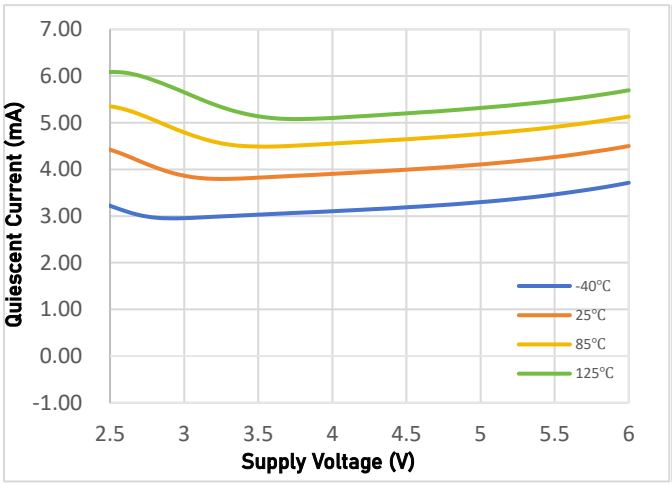


Figure 1: Quiescent Current vs Supply Voltage

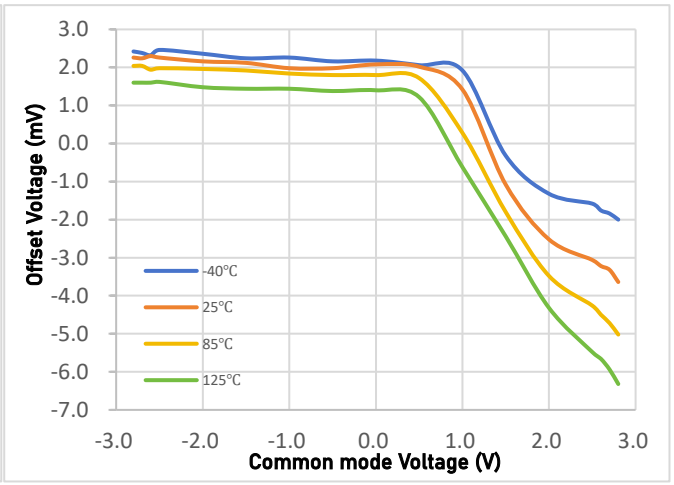


Figure 2: Offset Voltage vs Common mode Voltage

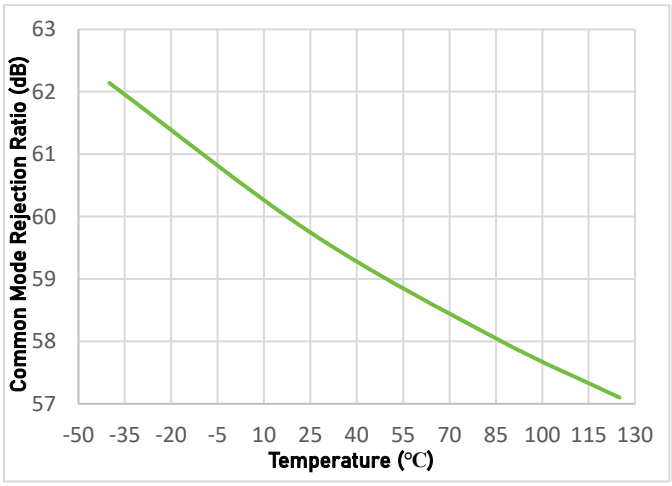


Figure 3: Common mode rejection ratio vs Temperature

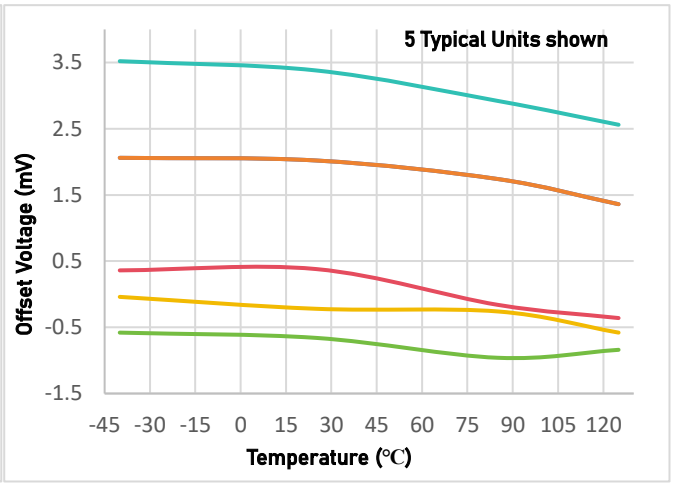


Figure 4: Offset Voltage vs Temperature

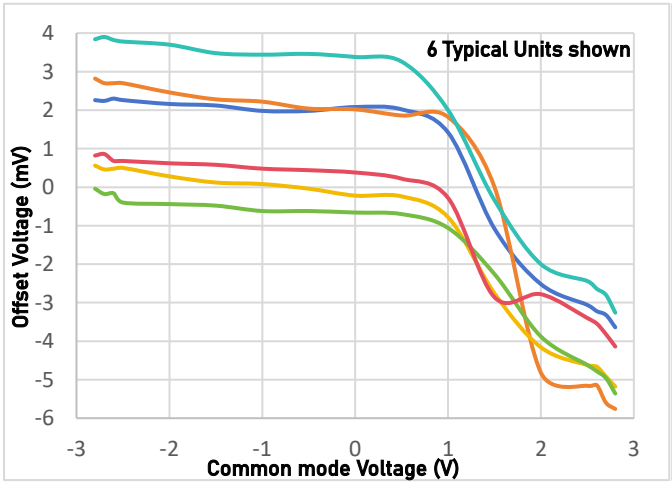


Figure 5: Offset Voltage vs Common mode Voltage

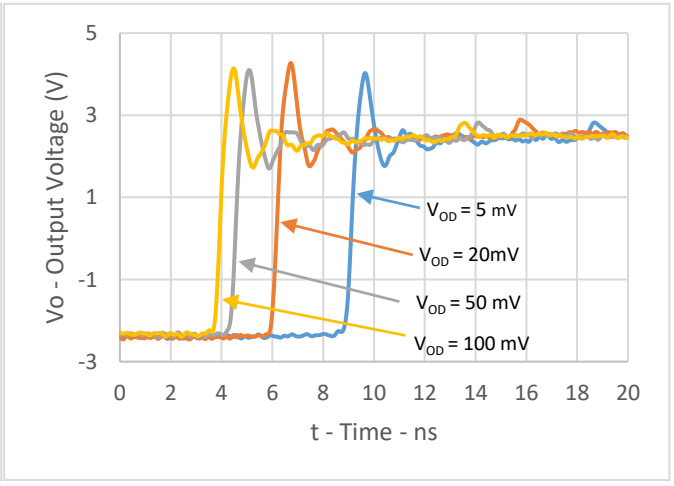


Figure 6: Propagation Delay Rising Edge

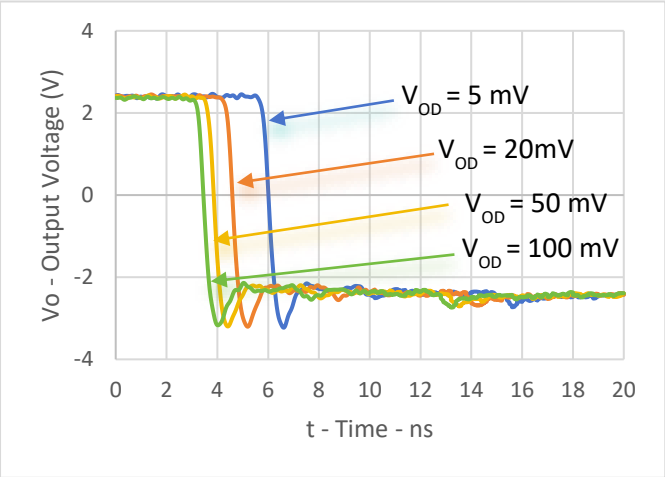


Figure 7: Propagation Delay Falling Edge

Detailed Description

Operating Voltage

The LTA677x family of micro-power push pull output comparators is fully specified and ensured for operation from 2.7 to 5.5V and offers an excellent speed-to-power combination with propagation delay of 4ns and a quiescent supply current of 3mA.This combination of fast response time at micro-power enables power conscious systems to monitor and respond quickly to fault conditions.

In addition, and many specifications apply over the industrial temperature range of -40℃ to +85℃, parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

Shutdown

A shutdown pin (LTA6771 only) allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws approximately TBD µA, and the output goes to high impedance. When the shutdown pin is low, the LTA6771 is active. When the LTA6771 shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in Figure 10. Exiting shutdown mode requires approximately TBD ns. The LTA6772 and LTA6773 do not have the shutdown feature.

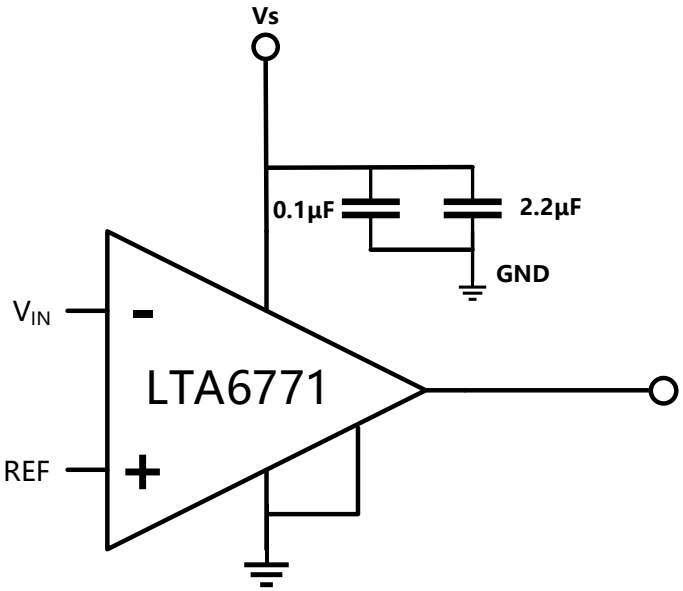


Figure 10: Basic connections for the LTA6771

Input Voltage

The LTA6771/6772/6773 comparator family uses CMOS transistors at the inputs which prevent phase inversion when the input pins exceed the supply voltages.

Internal ESD protection diodes (D1，D2，D3，and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

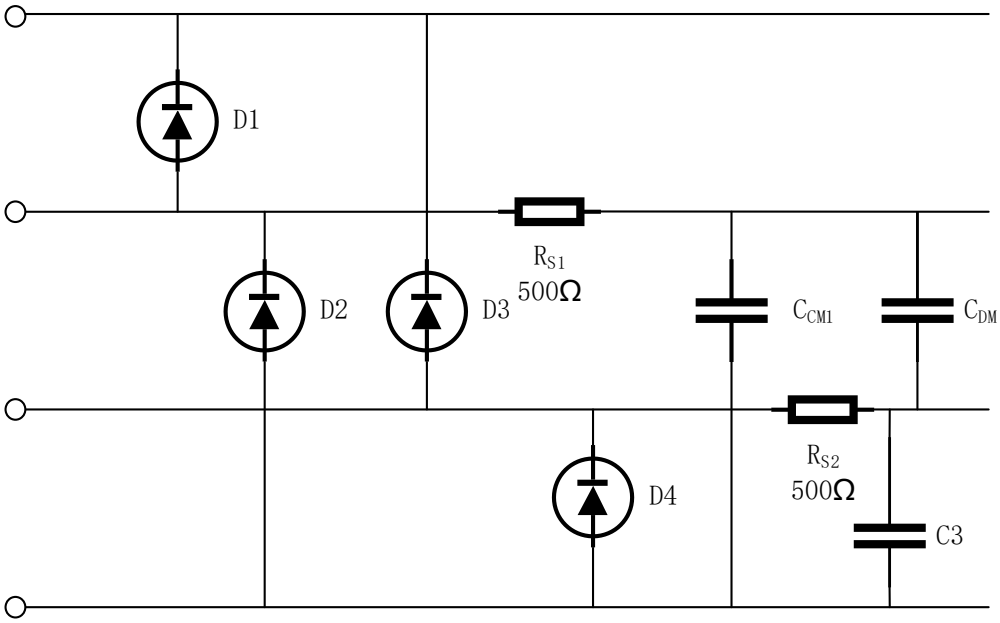


Figure 11: Input EMI Filter and Clamp Circuit

EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI.When the signal strength is low and transmission lines are long, an amplifier must accurately amplify the input signals. However, all comparator pins---the non-inverting input, positive supply, negative supply, and output pins---are susceptible to EMI signals. These high frequency signals are coupled into a comparator by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However,due to the nonlinearities of input devices, comparators can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LTA6771/6772/6773 comparators have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\log (V_{IN\_PEAK} / \Delta V_{OS})$$

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input.To counter the parasitic effects and noise,the devices have an internal hysteresis of 5mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. Figure 12 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

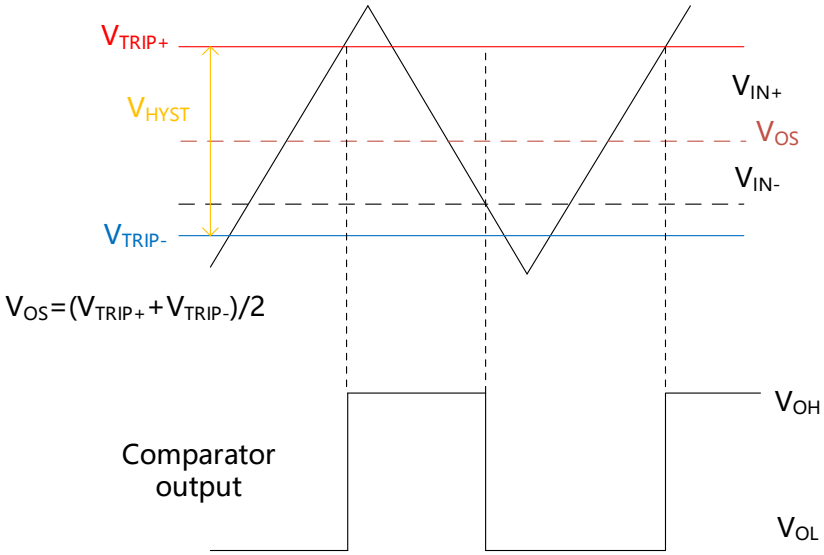


Figure 12. Input and Output waveform, Non-inverting input varied

Maximizing performance through proper layout

To achieve ths maximum performance of the extremely high input impedance and low offset voltage of the LTA6771/LTA6772/LTA6773 devices，care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier，reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 13 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermo-electric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

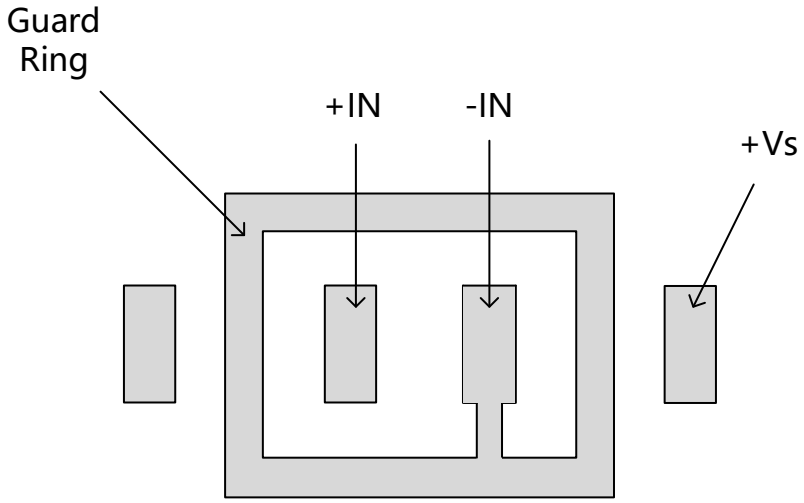


Figure 13: Use a guard ring around sensitive pins

Input and Output coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

Add Extenal Hysteresis

Inverting External Hysteresis

The LTA677x has robust performance when used with a good layout. However, the comparator input has almost no immunity in the range of a specific offset voltage (±5 mV). For slow moving or noisy input signals When the input signal moves past the switching threshold, the comparator output may cause an unwanted switching state. In such applications, the LTA677x's 10mV internal hysteresis may not be sufficient. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the non-inverting input.

Figure 14 shows a typical topology used to introduce additional hysteresis;

Figure 15 shows equivalent circuit when V_{OUT} switch from low to high;

Figure 16 shows equivalent circuit when V_{OUT} switch from high to low;

Use equation 1 to calculate Vtr (The voltage which let output switch from low to high) and use equation 2 to calculate Vtf (The voltage which let output switch from high to low); Finally the approximate total hysteresis could be calculated by using equation 3.

$$V_{tr} = \frac{(Vcc - Vref) * R2}{R1 + R2} + Vref \qquad (1)$$

$$V_{tf} = \frac{R1 * Vref}{R1 + R2} \qquad (2)$$

$$V_{HYST} = (Vtr\text{-}Vtf) + V_{HYST\text{-}INTL} = \frac{(V+)*R2}{(R1+R2)} + 10mV \qquad (3)$$

The total hysteresis, V_{HYST}, sets the value of the transition voltage required to switch the comparator output, by enlarging the threshold region, thereby reducing sensitivity to noise.

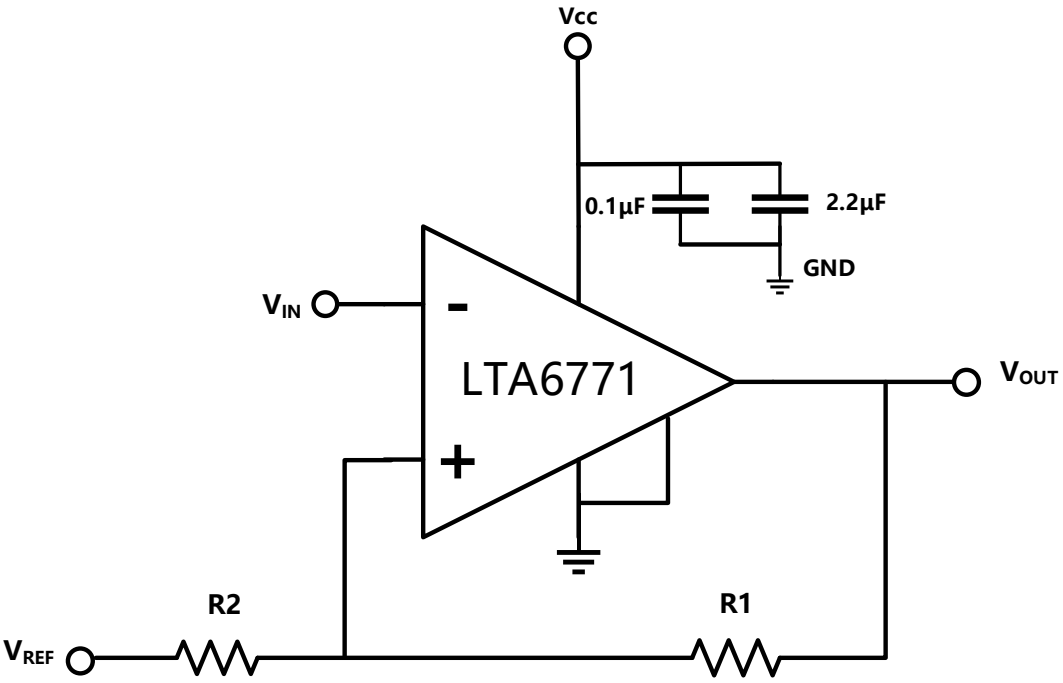


Figure 14: Adding External Hysteresis of LTA677x

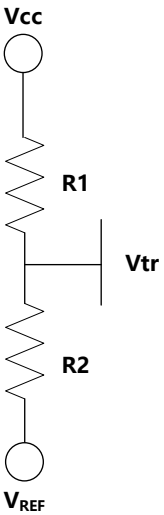


Figure 15: Equivalent circuit -- Vout from low to high

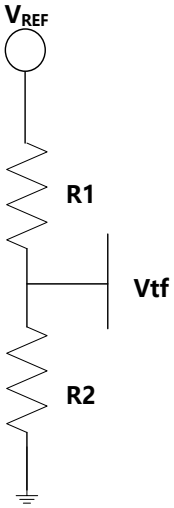


Figure 16: Equivalent circuit -- Vout from high to low

Non-Inverting External Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 17, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{tr}. V_{tr} is calculated by Equation 5

$$V_{ref} = \frac{R2}{R1+R2} * V_{cc} \qquad (4)$$

$$V_{tr} = \frac{Vref}{R3} * (R3 + R4) \qquad (5)$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} can be calculated by Equation 6. Finally the approximate total hysteresis could be calculated by using equation 7.

$$V_{tf} = \frac{Vref(R3+R4)-Vcc*R4}{R3} \quad (6)$$

$$V_{HYST} = (V_{tr}-V_{tf})+V_{HYST-INTL} = \frac{R4}{R3} * Vcc + 10mV \quad (7)$$

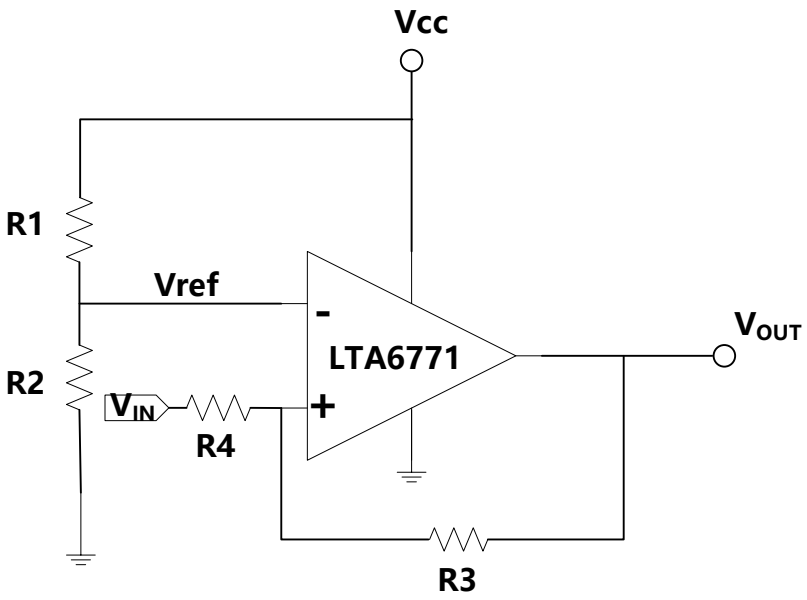


FIGURE 17: NON-INVERTING CONFIGURATION with Hysteresis

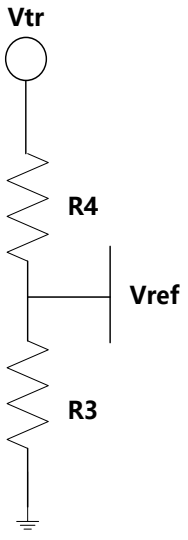


Figure 18: Equivalent circuit of Vin from low to high

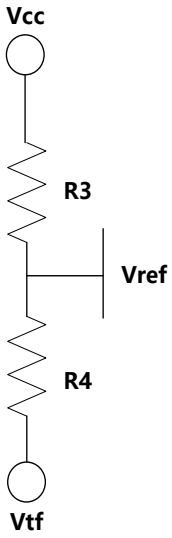


Figure 19: Equivalent circuit of Vin from high to low

IR Reciever AFE and Wake-Up Circuit

Infrared (IR) communication is inherently immune to RF interference as long as there is a line-of-sight path between the transmitter and the receiver. It is also one of the lowest cost communication schemes. This makes it a good choice for implementing wireless communications in applications such as utility metering. A common system topology to extend battery life is to use a power efficient IR receiver analog front end (AFE) that is always on and wakes up the host only when there is valid IR signal detected as shown in Figure 20.

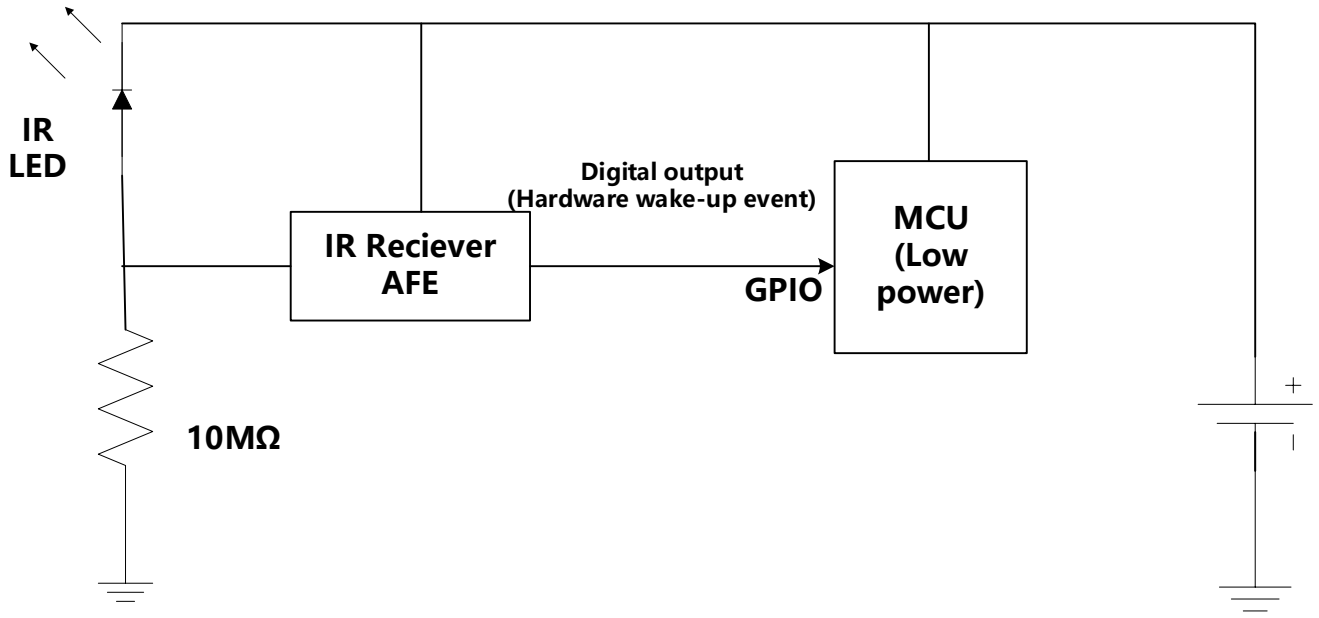


Figure 20: Coin Cell Battery Powered IR Receiver

Power efficient comparators such as the LTA677x can be used in the IR receiver AFE to increase battery life. The LTA677x device is responsible for two major tasks:

1. IR signal conditioning
2. Host system wake-up

LTA677x device is constantly powered to always be ready to receive IR signals and wake up the host microcontroller (MCU) when data is received. The short working distance (approximately 5cm) is suitable for a virtual-contact operation where the IR transmitter and receiver are closely placed with an optional mechanical alignment guide.

Figure 20 shows the IR receiver system block diagram. The host MCU is normally in the shutdown mode (during which the quiescent current is less than 1 μA) except when data is being transferred.

Figure 21 shows the detailed circuit design. The circuit established a threshold through R2 and C1 which automatically adapts to the ambient light level. To further reduce BOM cost, this example uses an IR LED as the IR receiver. The IR LED is reverse-biased to function as a photodiode (but at a reduced sensitivity).

The load resistor R1 converts the IR light induced current into a voltage fed into the inverting input of the comparator. R2 and C1 establish a reference voltage V_{REF} which tracks the mean amplitude of the IR signal. The non-inverting input is connected to V_{REF} through R3. And finally R3 and R4 are used to introduce additional hysteresis to keep the output of spurious toggles.

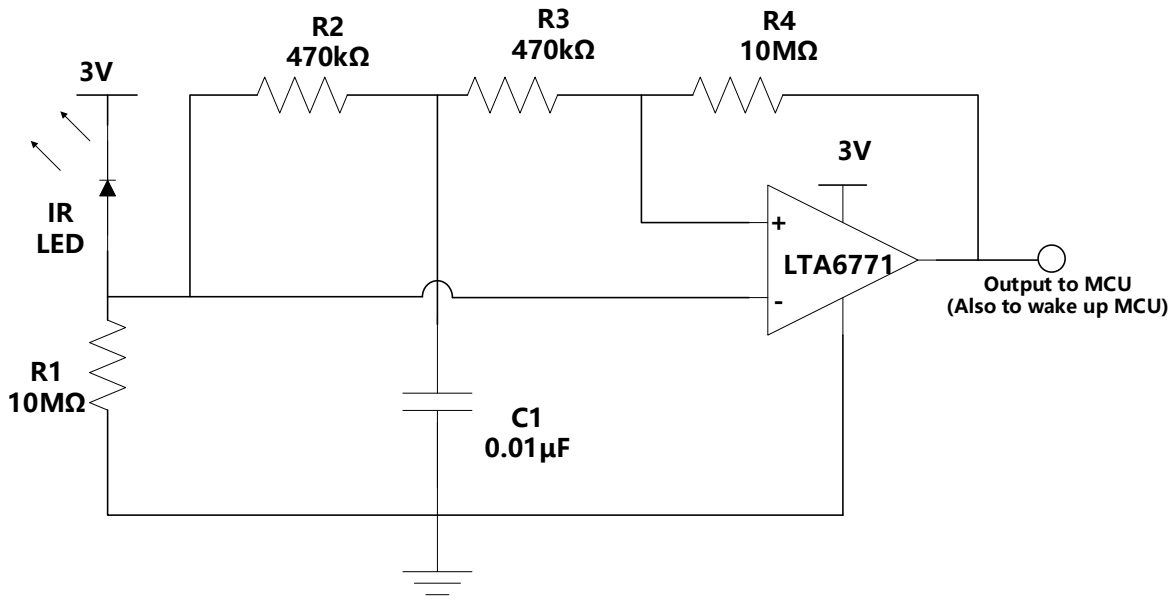


Figure 21: IR Receiver AFE using LTA6771

Window Comparator

Window Comparators are commonly used to detected undervoltage (UV) and overvoltage (OV) conditions. Figure 22 shows a simple window comparator circuit.

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3 V power supply

Configure the circuit as shown in Figure 22. Connect V_{S+} to a 3.3 V power supply and VS- to ground. Make R1, R2 and R3 each 10Mohm resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (VTH+ and VTH-). With each resistor being equal, VTH+ is 2.2 V and VTH- is 1.1 V. Large resistor values such as 10Mohm are used to minimize power consumption. The sensor output voltage is applied to the inverting and non-inverting inputs of the 2-channel LTA6772's. The respective comparator outputs will be low when the sensor is less than 1.1 V ot greater than 2.2 V. V_{OUT} will be high when the sensor is in the range of 1.1 V to 2.2 V. See the application curve in Figure 23.

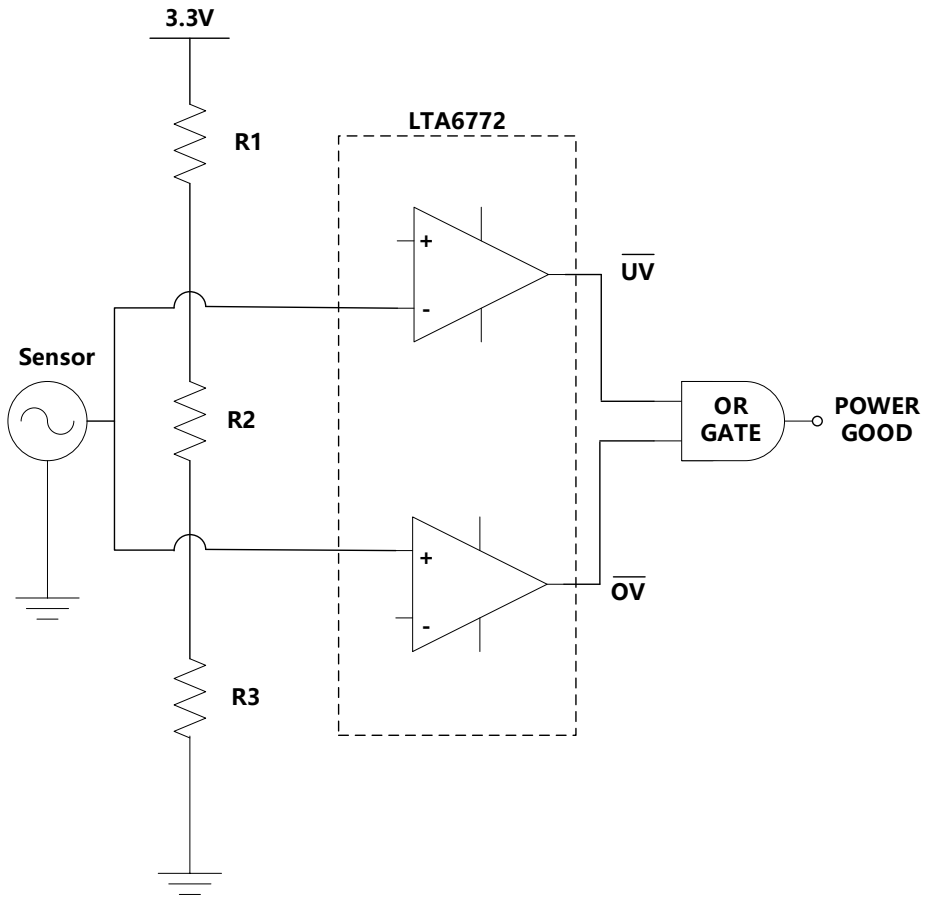


Figure 22: Window Comparator

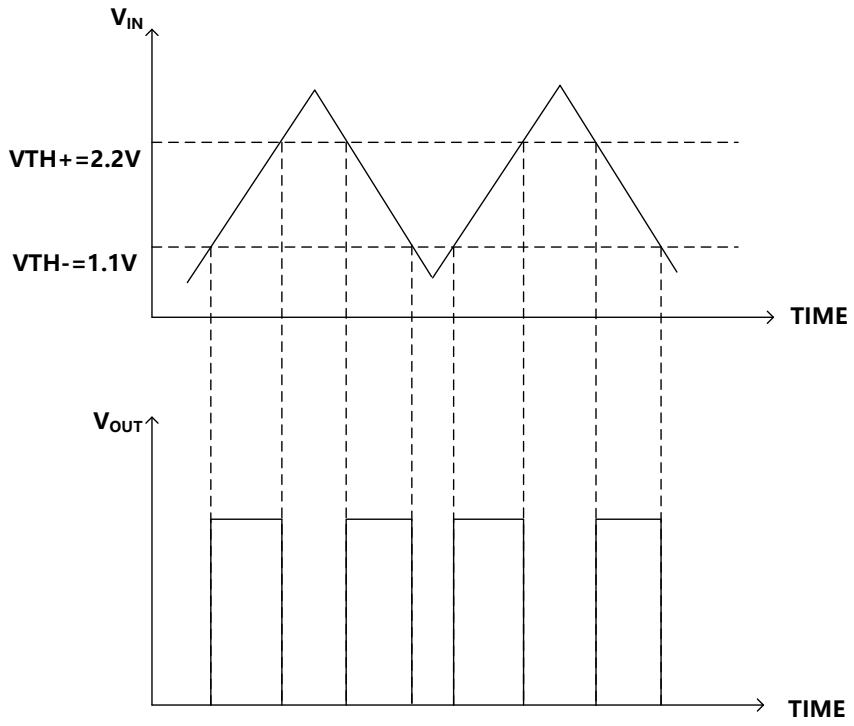
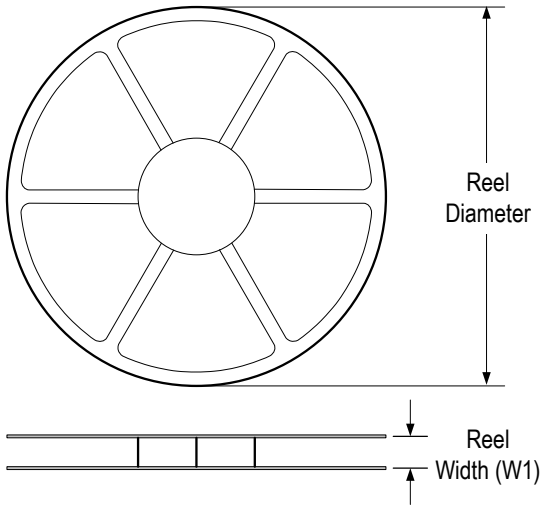


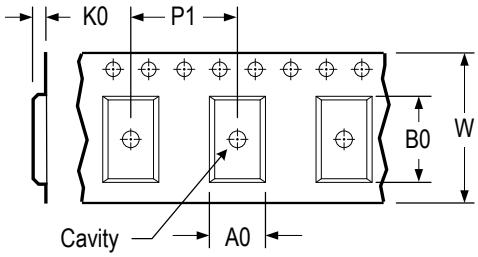
Figure 23: Window Comparator Results

Tape and Reel Information

REEL DIMENSIONS

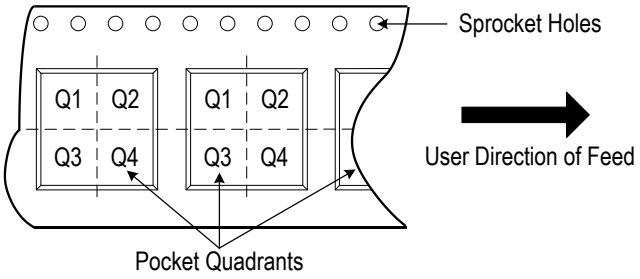


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

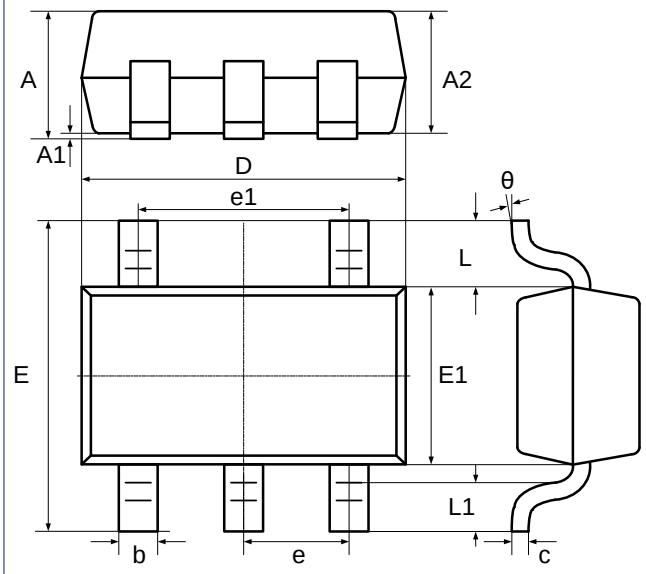


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA6771XT6/R6	SOT23	6	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA6771XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6772XT8S/R6	SOT23	8	3 000	330	12.4	4.0	3.2	1.5	4.0	8.0	Q1
LTA6772XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6772XV8/R6	MSOP	8	3 000	330	12.4	5.0	3.5	2.0	8.0	12.0	Q1
LTA6773XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA6773XC5/R6	SC70	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

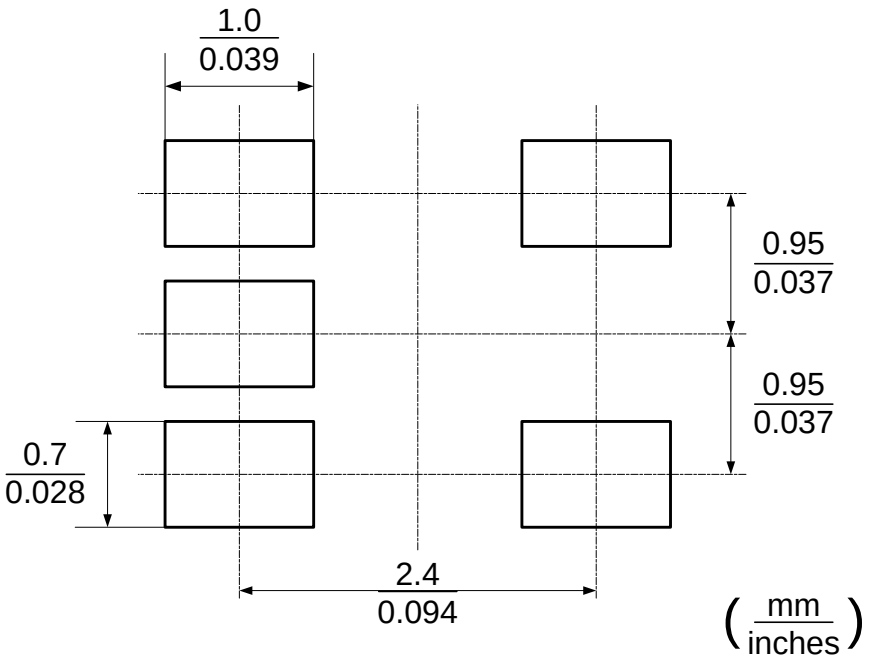
Package Outlines

DIMENSIONS, SOT23-5L



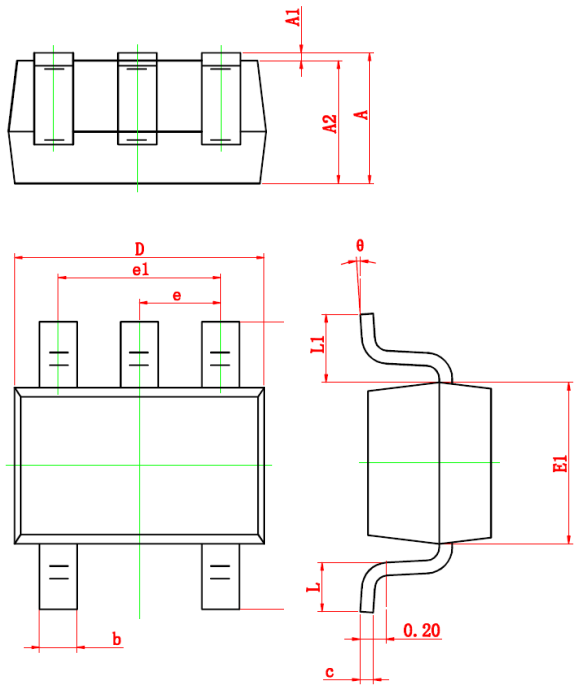
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



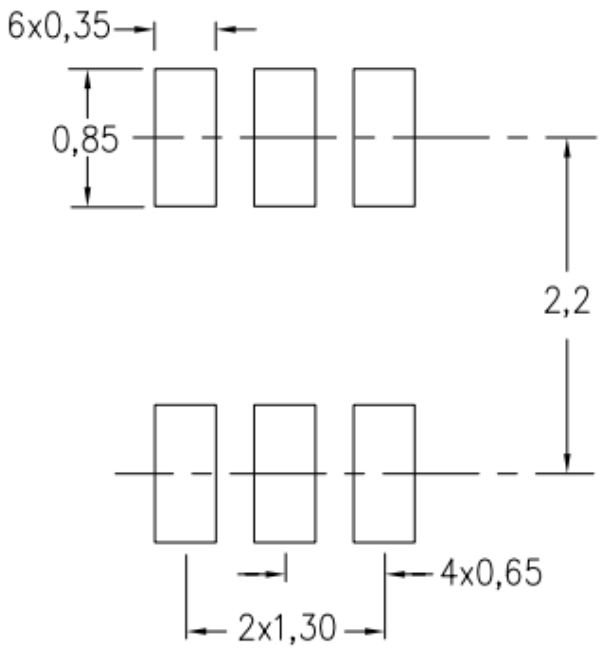
Package Outlines (Continued)

DIMENSIONS, SC70-5L



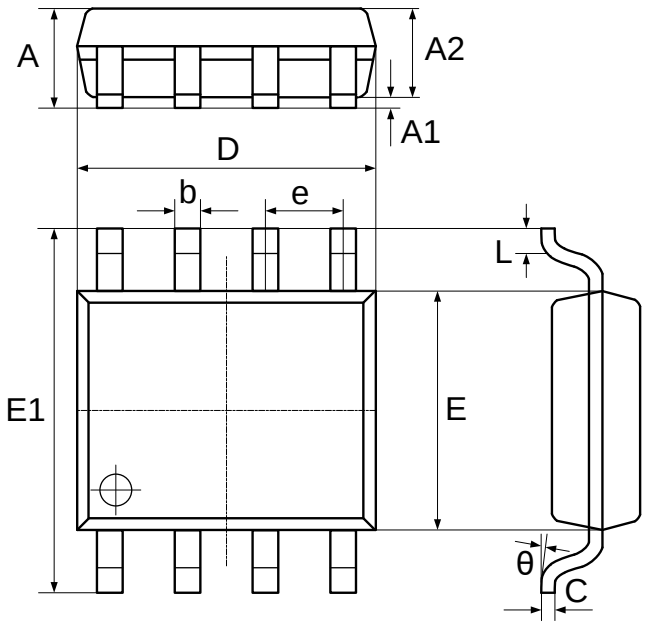
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650TYP		0.026REF	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525REF		0.021REF	
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SC70-5L



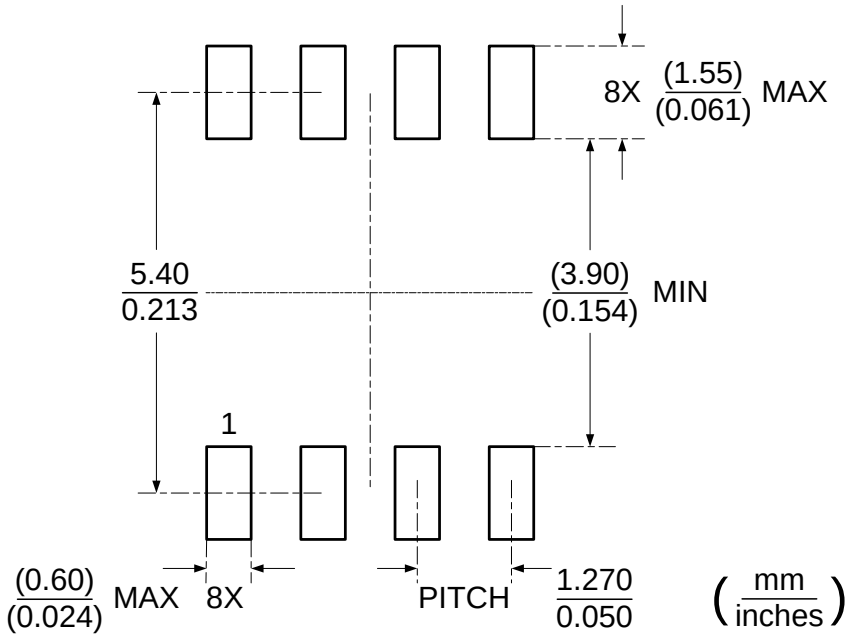
Package Outlines (Continued)

DIMENSIONS, SOIC-8L



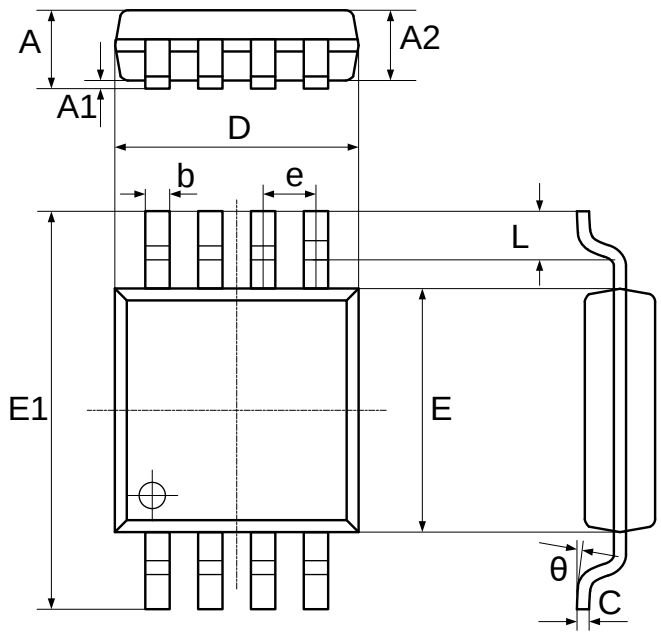
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



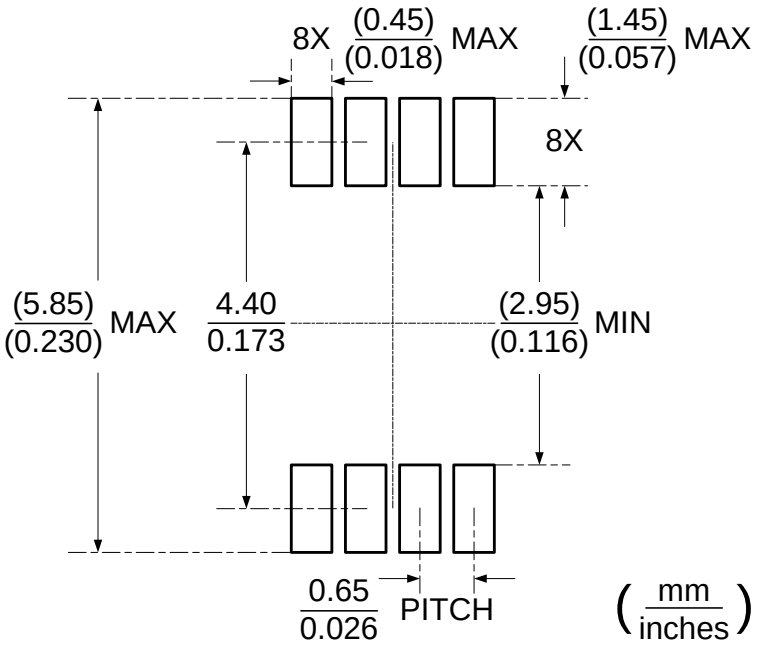
Package Outlines (Continued)

DIMENSIONS, MSOP-8L



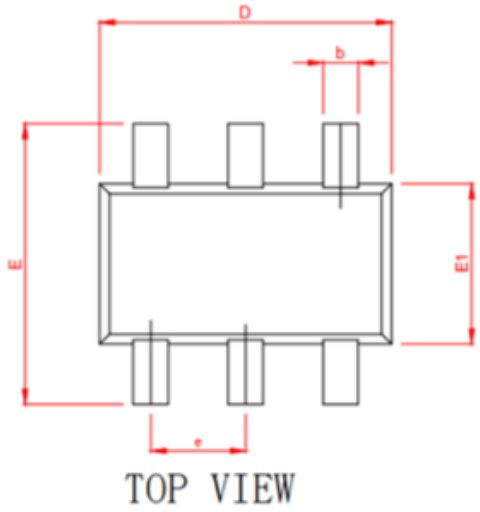
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

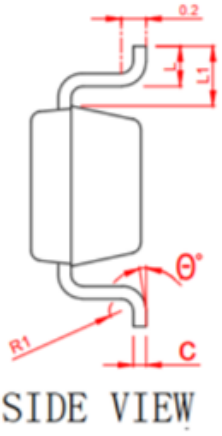
RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L

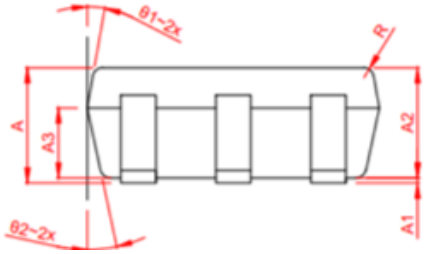


Package Outlines (Continued)

DIMENSIONS, SOT23-6L

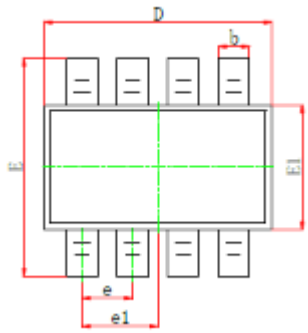


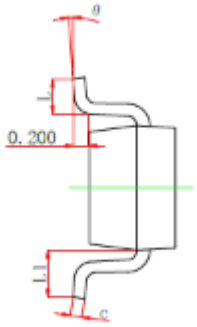


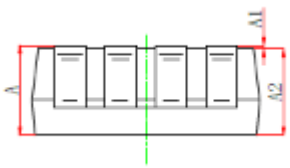


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.10	1.15	1.25
* A1	0.02	0.06	0.10
* A2	1.05	1.10	1.15
A3	0.60	0.65	0.70
* b	0.32	0.35	0.48
* c	0.152REF		
* D	2.87	2.92	2.97
* E	2.60	2.80	3.00
* E1	1.55	1.60	1.65
* e	0.95BSC		
* L	0.35	0.45	0.55
L1	0.60 REF		
R	0.10 REF		
R1	0.12 REF		
* θ	0°	3°	6°
θ1	7°BSC		
θ2	10°BSC		

DIMENSIONS, SOT23-8L







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.650BSC.		0.026BSC.	
e1	0.975BSC.		0.038BSC.	
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

Important Notice

Linearin is a global fabless semiconductor company specializing in advanced high-performance high-quality analog/mixed-signal IC products and sensor solutions. The company is devoted to the innovation of high performance, analog-intensive sensor front-end products and modular sensor solutions, applied in multi-market of medical & wearable devices, smart home, sensing of IoT, intelligent industrial & smart factory (industrial 4.0), and automotives. Linearin's product families include widely-used standard catalog products, solution-based application specific standard products (ASSPs) and sensor modules that help customers achieve faster time-to-market products. Go to http://www.linearin.com for a complete list of Linearin product families. For additional product information, or full datasheet, please contact with the Linearin's Sales Department or Representatives.