General Description

The LTP7693 is a low-noise (4 µVRMS), low-dropout linear regulator (LDO) capable of sourcing 3 A with only 200 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.15 V using an external resistor divider.

The combination of low-noise (4 µVRMS), high PSRR, and high output current capability makes the LTP7693 ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of the LTP7693 limits power-supply-generated phase noise and clock jitter, making this device ideal for powering high-performance serializer and deserializer (SerDes), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. Specifically, RF amplifiers benefit from the high-performance and 5.15 V output capability of the device.

For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs) requiring low-input voltage, low-output (LILO) voltage operation, the exceptional accuracy (±1% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the LTP7693 ensure optimal system performance.

The versatility of the LTP7693 makes the device a component of choice for many demanding applications.

Features

- Low dropout: 200 mV (max) at 3 A
- 1% (max) accuracy over line, load, and temperature
- Output voltage noise:
  - –4 µVRMS at 0.8 V output
  - –8.5 µVRMS at 5.15 V output
- Input voltage range:
  - –Without BIAS: 1.4 V to 6.5 V
  - –With BIAS: 1.1 V to 6.5 V
- ANY-OUT™ operation:
  - –Output voltage range: 0.8 V to 3.95 V
- Adjustable Output voltage range: 0.8 V to 5.15 V
- Power-supply ripple rejection: –40 dB at 500 kHz
- Excellent load transient response
- Adjustable soft-start in-rush control
- Open-drain power-good (PG) output
- Stable with a 47 µF or larger ceramic output capacitor
- Package：QFN3.5×3.5-20

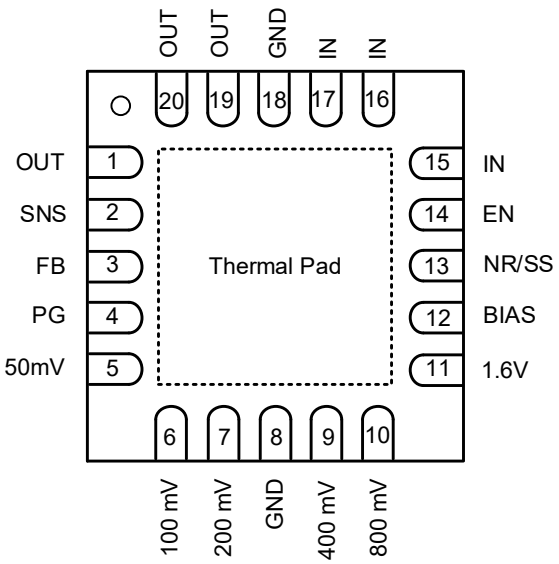
Applications

- Macro remote radio units (RRU)
- Outdoor backhaul units
- Active antenna system mMIMO (AAS)

Ordering Information

Model	Package	Ordering Number[Note1]	Packing Option
LTP7693	QFN3.5×3.5-20	LTP7693XF20/R10	Tape and Reel, 5 000

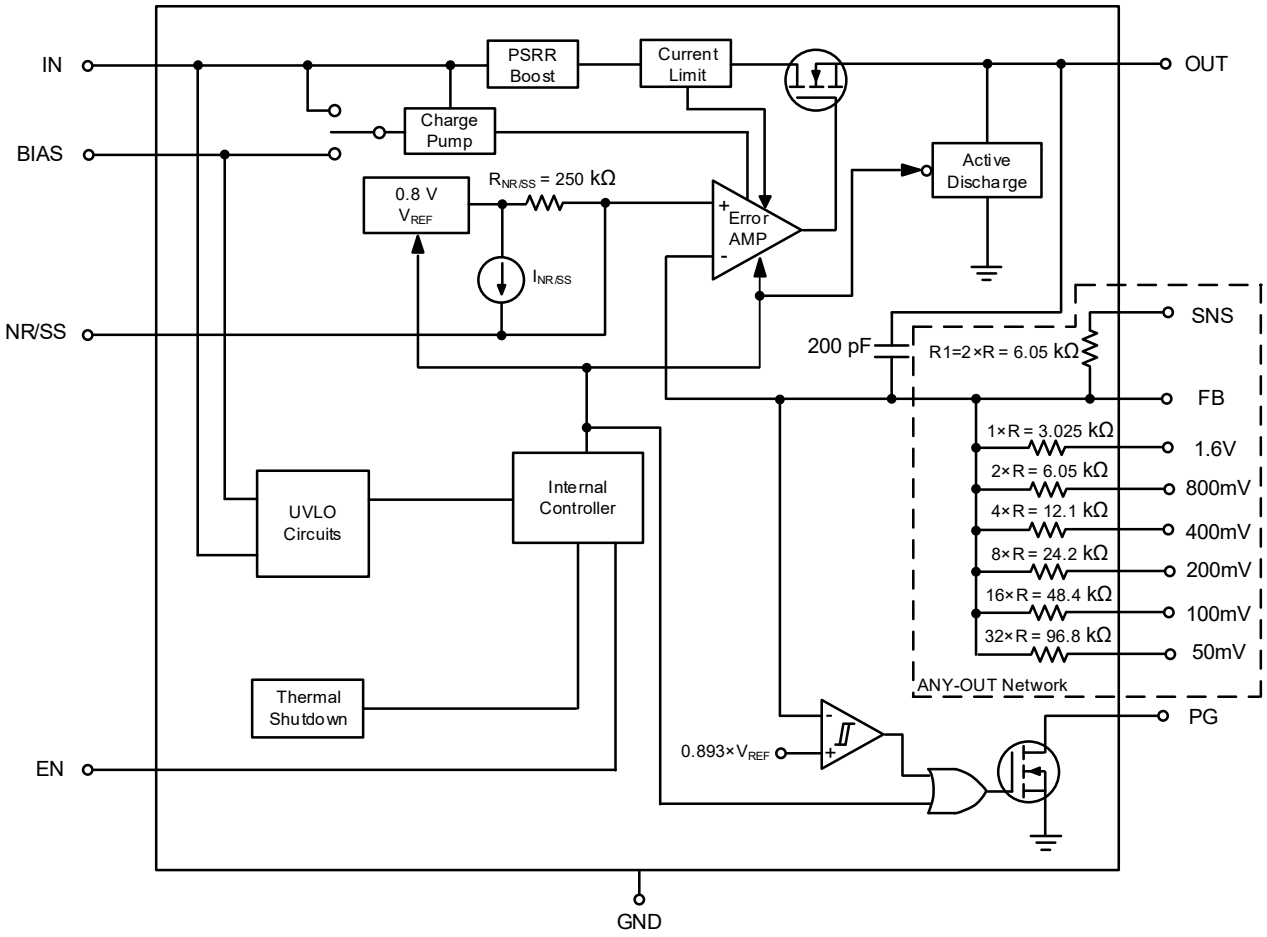
Pin Configurations (Top View)



Pin Function

Pin no.	Symbol	Function
5	50 mV	ANY-OUT voltage setting pins. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the ANY-OUT network but decreases the range of the network; multiple pins can be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use. See the ANY-OUT Programmable Output Voltage section for additional details.
6	100 mV	
7	200 mV	
9	400 mV	
10	800 mV	
11	1.6 V	
12	BIAS	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.2 V, V_{OUT} = 1 V) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for $V_{IN} \leq 2.2$ V. A 10 µF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
14	EN	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. If enable functionality is required, V_{EN} must always be high after V_{IN} is established when a BIAS supply is used.
3	FB	Feedback pin connected to the error amplifier. Although not required, a 10 nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize ac performance. The use of a feed-forward capacitor can disrupt PG (power good) functionality.
8,18	GND	Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.
15-17	IN	Input supply voltage pin. A 47-µF or larger ceramic capacitor (5 µF or greater of capacitance) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
13	NR/SS	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
1,19,20	OUT	Regulated output pin. A 47 µF or larger ceramic capacitor (25 µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
4	PG	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. The use of a feed-forward capacitor can disrupt PG (power good) functionality.
2	SNS	Output voltage sense input pin. This pin connects the internal R1 resistor to the output. Connect this pin to the load side of the output trace only if the ANY-OUT feature is used. If the ANY-OUT feature is not used, leave this pin floating. See the ANY-OUT Programmable Output Voltage and Adjustable Operation sections for more details.
	Thermal pad	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

Block Diagram



Functional Description

Low-Noise, High-PSRR Output

The LTP7693 includes a low-noise reference and error amplifier ensuring minimal noise during operation. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) are the easiest way to reduce device noise. $C_{NR/SS}$ filters the noise from the reference and C_{FF} filters the noise from the error amplifier. The noise contribution from the charge pump is minimal. The overall noise of the system at low output voltages can be reduced by using a bias rail because this rail provides more headroom for internal circuitry.

The high power-supply rejection ratio (PSRR) of the LTP7693 ensures minimal coupling of input supply noise to the output. The PSRR performance is primarily results from a high-bandwidth, high-gain error amplifier and an innovative circuit to boost the PSRR between 200 kHz and 1 MHz.

The combination of a low noise-floor and high PSRR ensure that the device provides a clean supply to the application; see the Optimizing Noise and PSRR section for more information on optimizing the noise and PSRR performance.

Integrated Resistance Network (ANY-OUT)

An internal feedback resistance network is provided, allowing the LTP7693 output voltage to be programmed easily between 0.8 V to 3.95 V with a 50 mV step by tying the ANY-OUT pins to ground. Tying the ANY-OUT pins to SNS increases the resolution but limits the range of the output voltage because the effective value of R1s decreased. Use the ANY-OUT network for excellent accuracy across output voltage and temperature;

Bias Rail

The device features a bias rail to enable low-input voltage, low-output (LILO) voltage operation by providing power to the internal circuitry of the device. The bias rail is required for operation with V_{IN} < 1.4 V.

An internal power MUX supplies the greater of either the input voltage or the bias voltage to an internal charge pump to power the internal circuitry. Unlike other LDOs that have a bias supply, the LTP7693 does not have a minimum bias voltage with respect to the input supply because an internal charge pump is used instead.

The internal charge pump multiples the output voltage of the power MUX by a factor of 4 to a maximum of typically 8 V; therefore, using a bias supply with $V_{IN} \leq 2.2$ V is recommended for optimal dc and ac performance. Sequencing requirements exist for when the bias rail is used;

Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage $V_{IT(PG)}$, typically 88%), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{IT(PG)}$, $+V_{HYS(PG)}$ (typically 90%), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended. Using an external voltage detector device is recommended in applications where more accurate voltage monitoring or overvoltage monitoring is required.

The use of a feed-forward capacitor (C_{FF}) can cause glitches on start-up, and the power-good circuit may not function normally below the minimum input supply range.

Functional Description

Programmable Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltages. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp time during turn-on. The start-up ramp is monotonic.

The majority of the ramp is linear; however, there is an offset voltage in the error amplifier that can cause a small initial jump in output voltage;

Internal Current Limit (I_{LIM})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

The foldback current limit crosses 0 A when V_{OUT} < 0 V and prevents the device from turning on into a negatively-biased output. See the Negatively-Biased Output section on additional ways to ensure start-up when the LTP7693 output is pulled below ground.

If V_{OUT} > V_{IN} + 0.3 V, then reverse current can flow from the output to the input. The reverse current can cause damage to the device; therefore, limit this reverse current to 10% of the rated output current of the device. See the Reverse Current Protection section for more details.

Enable

The enable pin for the LTP7693 is active high. The output of the LTP7693 is turned on when the enable pin voltage is greater than its rising voltage threshold (1.1 V, max), and the output of the LTP7693 is turned off when the enable pin voltage is less than its falling voltage threshold (0.5 V, min). A voltage less than 0.5 V on the enable pin disables all internal circuits. At the next turn-on this voltage ensures a normal start-up waveform with in-rush control, provided there is enough time to discharge the output capacitance.

When the enable functionality is not desired, EN must be tied to V_{IN}. However, when the enable functionality is desired, the enable voltage must come after V_{IN} is above $V_{UVLO1(IN)}$ when a BIAS rail is used. See the Application and Implementation section for further details.

Active Discharge Circuit

The LTP7693 has an internal pulldown MOSFET that connects a resistance of several hundred ohms to ground when the device is disabled to actively discharge the output voltage when the device is disabled.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent the device from turning on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also disables the output of the device when V_{IN} or V_{BIAS} fall below the lockout voltage. The UVLO circuit responds quickly to glitches on V_{IN} or V_{BIAS} and attempts to disable the output of the device if either of these rails collapse. As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient.

Functional Description

Thermal Protection

The LTP7693 contains a thermal shutdown protection circuit to disable the device when thermal junction temperature (T_J) of the main pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to 140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C can cause the device to exceed its operational specifications. Although the internal protection circuitry of the LTP7693 is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the LTP7693 into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

Device Functional Modes

Operation with 1.1 V ≤ V_{IN} < 1.4 V

The LTP7693 requires a bias voltage on the BIAS pin greater than or equal to 3.0 V if the high-current input supply voltage is between 1.1 V to 1.4 V. The bias voltage pin consumes 2.4 mA, nominally.

Operation with 1.4 V ≤ V_{IN} ≤ 6.5 V

If the input voltage is equal to or exceeds 1.4 V, no BIAS voltage is required. The LTP7693 is powered from either the input supply or the BIAS supply, whichever is greater. For higher performance, a BIAS rail is recommended for V_{IN} ≤ 2.2 V.

Shutdown

Shutting down the device reduces the ground current of the device to a maximum of 25 µA.

Absolute Maximum Ratings

Parameter	Symbol	Rating or Value	Unit
IN, BIAS, PG, EN Voltage		-0.3 to 7.0	V
IN, BIAS, PG, EN Voltage (5% duty cycle, pulse duration = 200 µs)		-0.3 to 7.5	
SNS, OUT Voltage		-0.3 to V_{IN}+0.3	
NR/SS, FB Voltage		-0.3 to 3.6	
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V Voltage		-0.3 to V_{OUT}+0.3	
OUT Current		Internally limited	A
PG Current (sink current into device)		5	mA
Maximum Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Human Body Model	ESD	±2000	V
Charged-device model		±500	V

NOTE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The absolute maximum rating is VIN + 0.3 V or 7.0 V, whichever is smaller.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max	Unit
Input supply voltage range	V_{IN}	1.1		6.5	V
Bias supply voltage range(1)	V_{BIAS}	3		6.5	V
Output voltage range(2)	V_{OUT}	0.8		5.15	V
Enable voltage range	V_{EN}	0		Vin	V
Output current	I_{OUT}	0		3	A
Input capacitor	C_{IN}	10	47		µF
Output capacitor	C_{OUT}	47	47 || 10 || 10(3)		µF
Power-good pullup resistance	R_{PG}	10		100	kΩ
NR/SS capacitor	$C_{NR/SS}$		10		nF
Feed-forward capacitor	C_{FF}		10		nF
Top resistor value in feedback network for adjustable operation	R_1		6.05 (4)		kΩ
Bottom resistor value in feedback network for adjustable operation	R_2			160 (5)	kΩ
Operating junction temperature	T_J	-40		125	°C

NOTE:

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is required when the VIN supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN} \leq 2.2$ V.

(2) This output voltage range does not include device accuracy or accuracy of the feedback resistors.

(3) The recommended output capacitors are selected to optimize PSRR for the frequency range of 400 kHz to 700 kHz. This frequency range is a typical value for dc-dc supplies.

(4) The 6.05 kΩ resistor is selected to optimize PSRR and noise by matching the internal R1 value.

(5) The upper limit for the R2 resistor is to ensure accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

Caution

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. LINEARIN recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

LINEARIN reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact LINEARIN sales office to get the latest datasheet.

Electrical Characteristics: General

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V(1), OUT connected to 50 Ω to GND(2), V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ. Unless otherwise noted, typical values are at T_J = 25°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input supply UVLO with BIAS	$V_{UVLO1(IN)}$	V_{IN} rising with V_{BIAS} = 3.0 V		1.0	1.085	V
$V_{UVLO1(IN)}$ hysteresis	$V_{HYS1(IN)}$	V_{BIAS} = 3.0 V		200		mV
Input supply UVLO without BIAS	$V_{UVLO2(IN)}$	V_{IN} rising		1.31	1.39	V
$V_{UVLO2(IN)}$ hysteresis	$V_{HYS2(IN)}$			200		mV
Bias supply UVLO	$V_{UVLO(BIAS)}$	V_{BIAS} rising, V_{IN} = 1.1 V		2.89	3	V
$V_{UVLO(BIAS)}$ hysteresis	$V_{HYS(BIAS)}$	V_{IN} = 1.1 V		300		mV
EN Pin Input Current	I_{EN}	V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V	-0.1		0.1	µA
BIAS pin current	I_{BIAS}	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(nom)}$ = 0.8 V, I_{OUT} = 3 A		2.4	3.5	mA
EN pin low-level input voltage (disable device)	$V_{IL(EN)}$		0		0.5	V
EN pin high-level input voltage (enable device)	$V_{IH(EN)}$		1.1		6.5	V
PG pin low-level output voltage	$V_{OL(PG)}$	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
PG pin leakage current	$I_{lkg(PG)}$	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5 V			1	µA
NR/SS pin charging current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5 V	2	6.6	9	µA
FB pin leakage current	I_{FB}	V_{IN} = 6.5 V	-100		100	nA
Thermal shutdown temperature	T_{sd}	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
Operating junction temperature	T_J		-40		125	°C

Note:

(1) $V_{OUT(nom)}$ is the calculated VOUT target value from the ANY-OUT in a fixed configuration. In an adjustable configuration, $V_{OUT(nom)}$ is the expected V_{OUT} value set by the external feedback resistors.

(2) This 50 Ω load is disconnected when the test conditions specify an I_{OUT} value.

Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ. Unless otherwise noted, typical values are at T_J = 25°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage Operation Range	V_{IN}		1.1		6.5	V
Bias supply voltage range(1)	V_{BIAS}	V_{IN} = 1.1 V	3.0		6.5	V
Feedback voltage	V_{FB}			0.8		V
NR/SS pin voltage	$V_{NR/SS}$			0.8		V
Output Voltage Range	V_{OUT}	Using the ANY-OUT pins	0.8–1.0%		3.95+1.0%	V
		Using external resistors(2)	0.8–1.0%		5.15+1.0%	V
Output Voltage Accuracy(3)		0.8 V ≤ V_{OUT} ≤ 5.15 V, 5 mA ≤ I_{OUT} ≤ 3A, over V_{IN}	-1%		1%	
Output Voltage Accuracy With BIAS		V_{IN} = 1.1 V, 5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V	-0.75%		0.75%	
Line Regulation	ΔVO(ΔVI)	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.03		mV/V
Load Regulation	ΔVO(ΔIO)	5 mA ≤ I_{OUT} ≤ 3 A, 3.0 V ≤ V_{BIAS} ≤ 6.5 V, V_{IN} = 1.1 V		0.5		mV/A
		5 mA ≤ I_{OUT} ≤ 3 A		0.4		
		5 mA ≤ I_{OUT} ≤ 3 A, V_{OUT} = 5.15 V		2.5		
Dropout Voltage	V_{DO}	V_{OUT} = 1.1 V, I_{OUT} = 3 A		140	250	mV
		V_{OUT} = 3.3 V, I_{OUT} = 3 A		170	300	
		V_{OUT} = 5 V, I_{OUT} = 3 A		200	340	
Output Current Limit	I_{LIM}	V_{OUT} = 90%$V_{OUT-NOM}$, V_{IN} = $V_{OUT(nom)}$ + 0.4 V		4.2	5.2	A
Short-circuit current limit	I_{SC}	R_{LOAD} = 20 mΩ		2		A
Power-supply ripple rejection	PSRR	V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} =47 µF || 10 µF || 10 µF; f = 10 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		40		dB
		f = 500 kHz, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V		40		
		f = 10 kHz, V_{OUT} = 5.0 V		38		
		f = 500 kHz, V_{OUT} = 5.0 V		22		
Output noise voltage	V_n	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF		4		$µV_{RMS}$
		BW = 10 Hz to 100 kHz, V_{OUT} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF		8.5		
GND pin current	I_{GND}	V_{IN} = 6.5 V, I_{OUT} = 5 mA		3	4	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		4.3	5.5	
		Shutdown, PG = open, V_{IN} = 6.5 V, V_{EN} = 0.5 V		1.2	25	µA

Electrical Characteristics

Over operating junction temperature range (T_J = −40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ. Unless otherwise noted, typical values are at T_J = 25°C.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PG pin threshold	$V_{IT(PG)}$	For falling V_{OUT}	82%V_{OUT}	88%V_{OUT}	93%V_{OUT}	V
PG pin hysteresis	$V_{HYS(PG)}$	For rising V_{OUT}		2%V_{OUT}		V

Note:

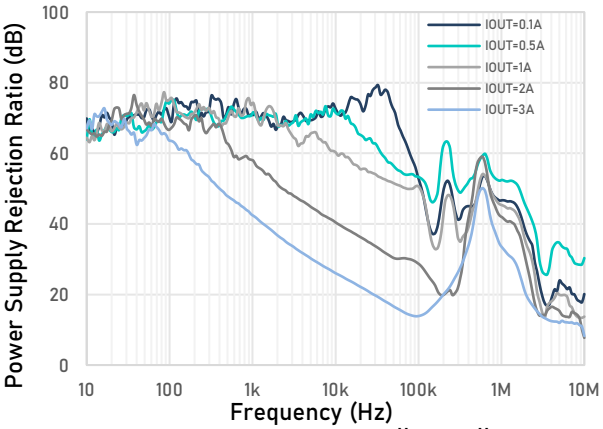
(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is required when the V_{IN} supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for $V_{IN} \leq$ 2.2 V.

(2) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

(3) The device is not tested under conditions where $V_{IN} > V_{OUT}$ + 1.7 V and I_{OUT} = 3 A, because the power dissipation is higher than the maximum rating of the package.

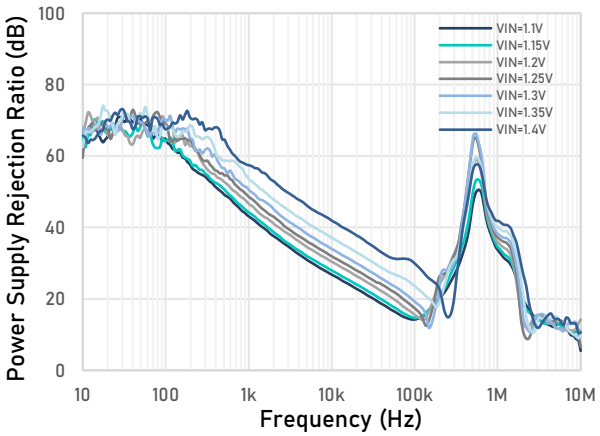
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



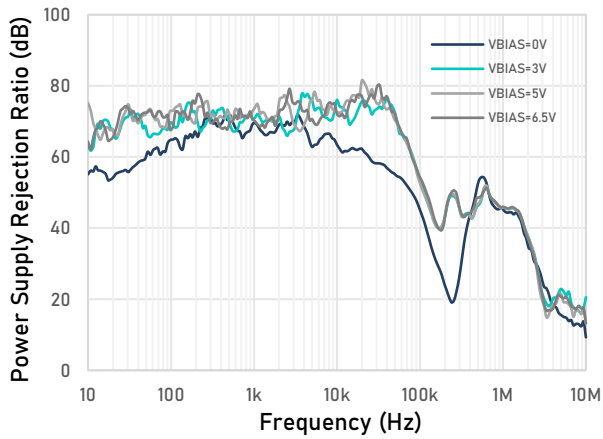
V_{IN} = 1.1 V, V_{BIAS} = 5 V, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig1. PSRR vs Frequency and I_{OUT}



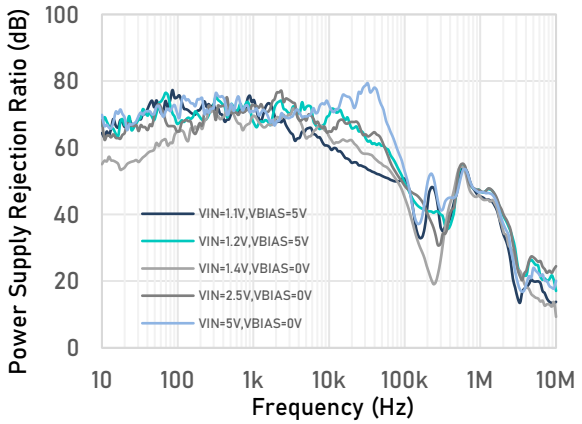
I_{OUT} = 3 A, V_{BIAS} = 5 V, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig2. PSRR vs Frequency and I_{IN} With Bias



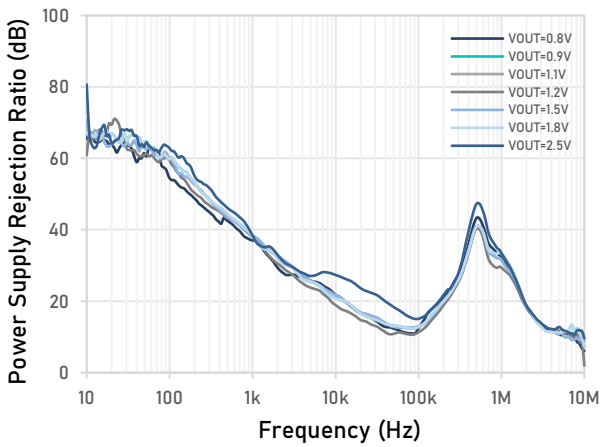
V_{IN} = 1.4 V, I_{OUT} = 1 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig3. PSRR vs Frequency and V_{BIAS}



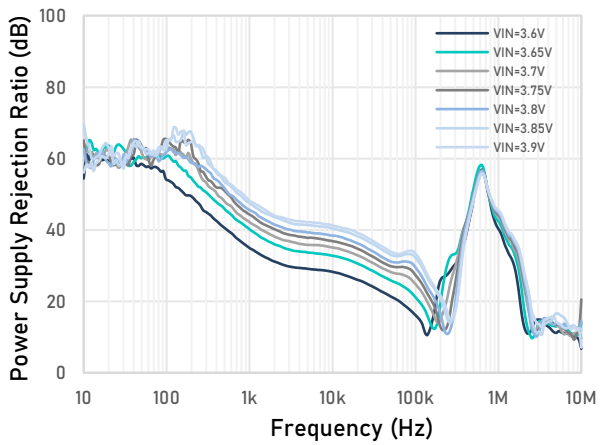
I_{OUT} = 1 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig4. PSRR vs Frequency and V_{IN}



V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig5. PSRR vs Frequency and V_{OUT} With Bias

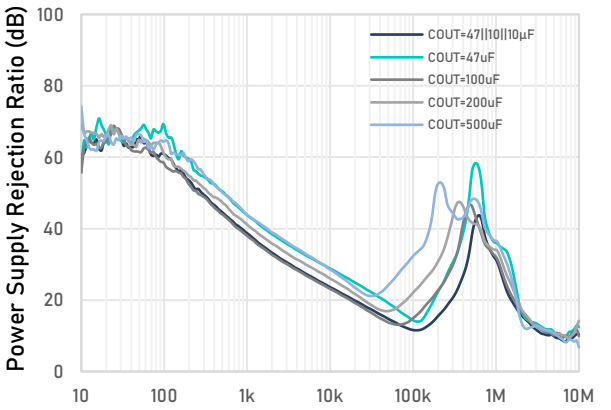


I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig6. PSRR vs Frequency and V_{IN} for V_{OUT} = 3.3 V

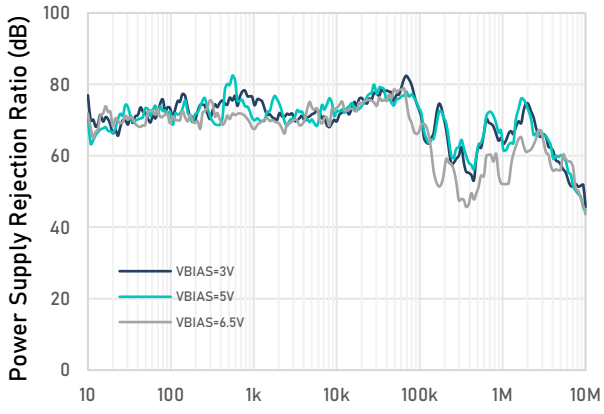
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



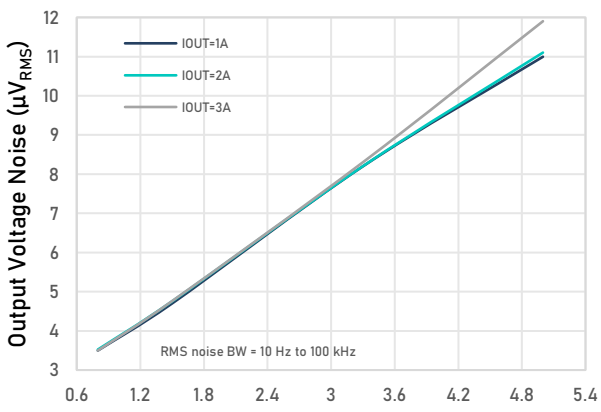
V_{IN} = 1.4V , V_{BIAS} = 5 V, V_{OUT} = 1 V, I_{OUT} = 3 A
$C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig7. PSRR vs Frequency and C_{OUT}



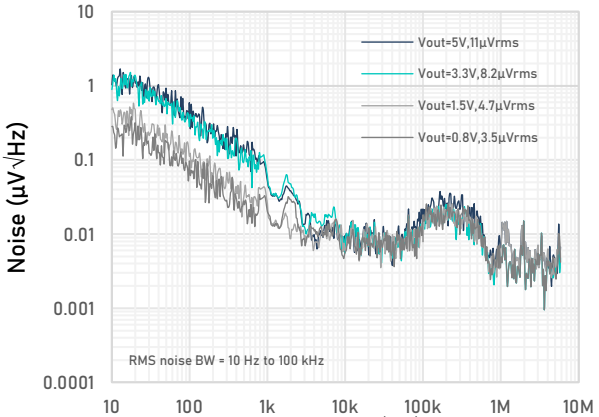
V_{IN} = V_{OUT} + 0.3 V, V_{OUT} = 1 V, I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig8. V_{BIAS} PSRR vs Frequency



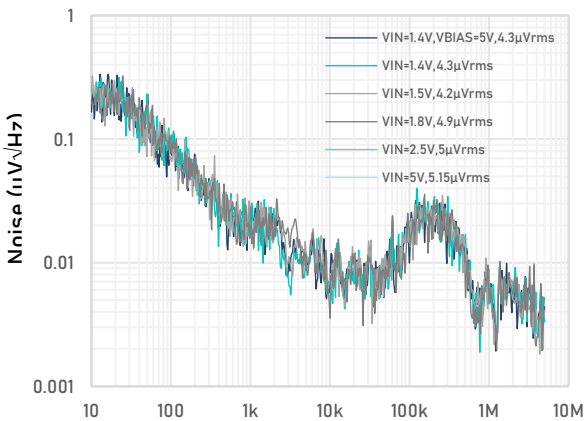
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Fig9. Output Voltage Noise vs Output Voltage



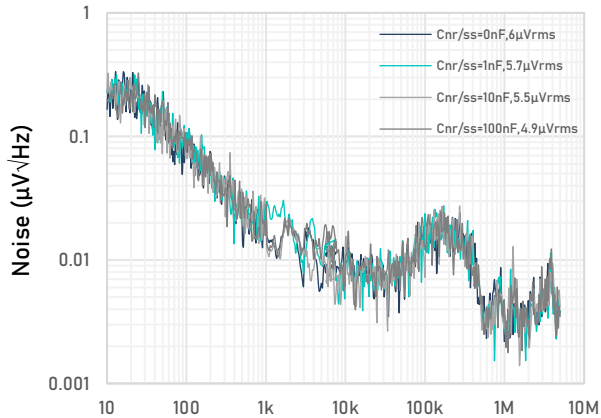
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V for V_{OUT} ≤ 2.2 V, I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF,

Fig10. Output Noise vs Frequency and Output Voltage



I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

Fig11. Output Noise vs Frequency and Input Voltage

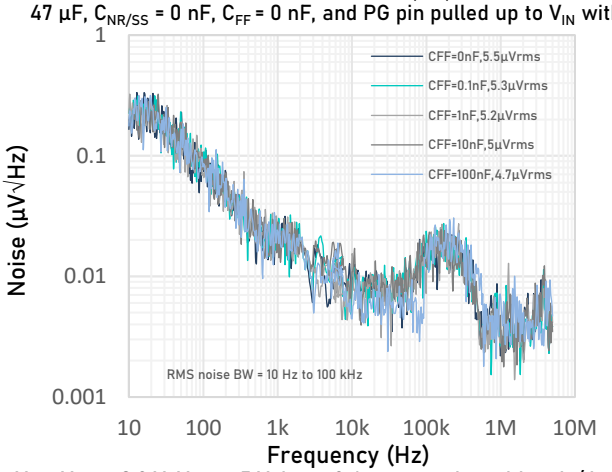


V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

Fig12. Output Noise vs Frequency and $C_{NR/SS}$

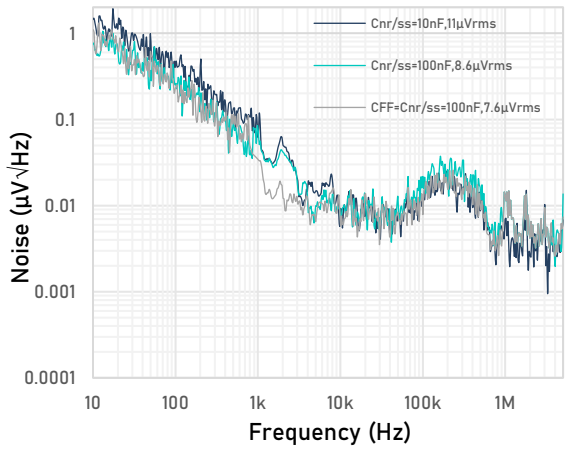
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



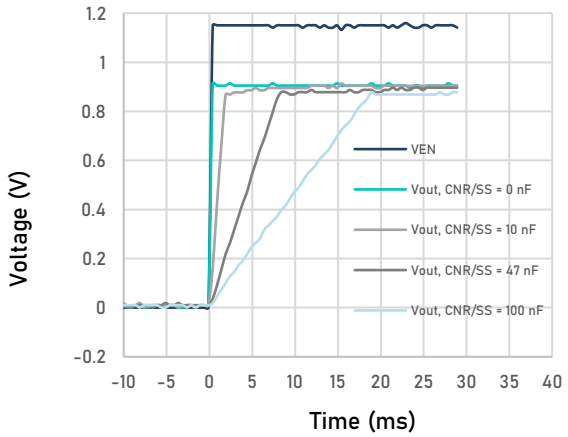
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, sequencing with a dc/dc converter and PG, C_{OUT} = 47 uF || 10 uF || 10 uF, $C_{NR/SS}$ = 10 nF,

Fig13. Output Noise vs Frequency and C_{FF}



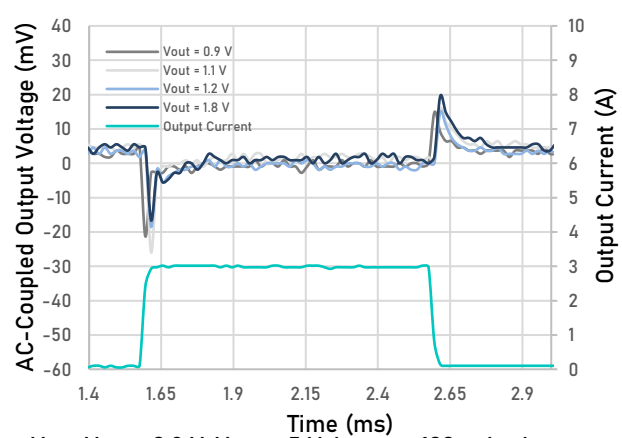
I_{OUT} = 3 A, C_{OUT} = 47 uF || 10 uF || 10 uF, C_{FF} = 10 nF, RMS noise BW = 10 Hz to 100 kHz

Fig14. Output Noise at 5 V Output



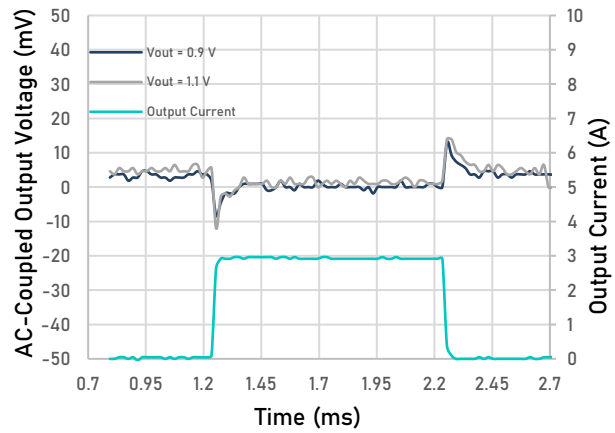
V_{IN} = 1.2 V, V_{OUT} = 0.9 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, C_{OUT} = 47 µF || 10 µF || 10 µF, C_{FF} = 10 nF

Fig15. Start-Up Waveform vs Time and $C_{NR/SS}$



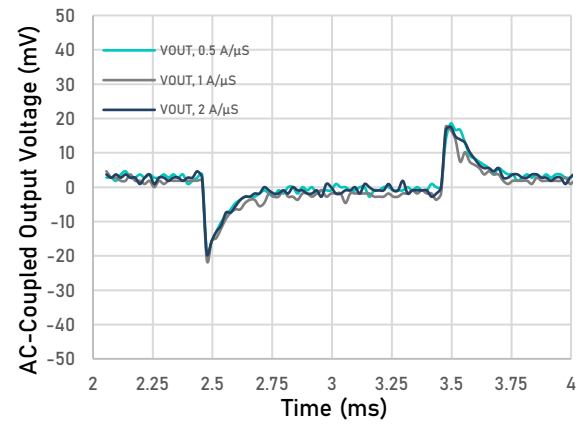
V_{IN} = V_{OUT} + 0.3 V, V_{BIAS} = 5 V, $I_{OUT, DC}$ = 100 mA, slew rate = 1 A/µs, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

Fig16. Load Transient vs Time and V_{OUT} With Bias



$I_{OUT, DC}$ = 100 mA, slew rate = 1 A/µs, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

Fig17. Load Transient vs Time and V_{OUT} Without Bias

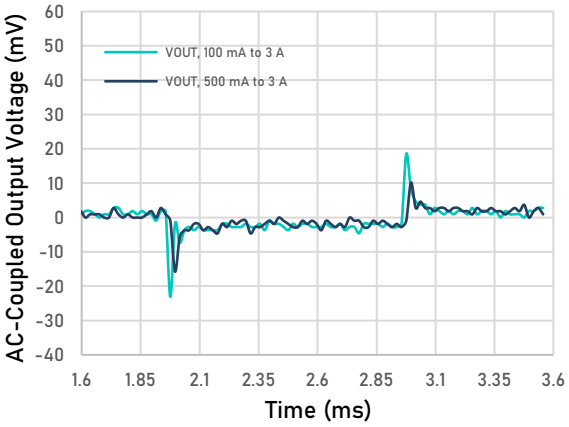


V_{OUT} = 5 V, $I_{OUT, DC}$ = 100 mA, I_{OUT} = 100 mA to 3 A, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

Fig18. Load Transient vs Time and Slew Rate

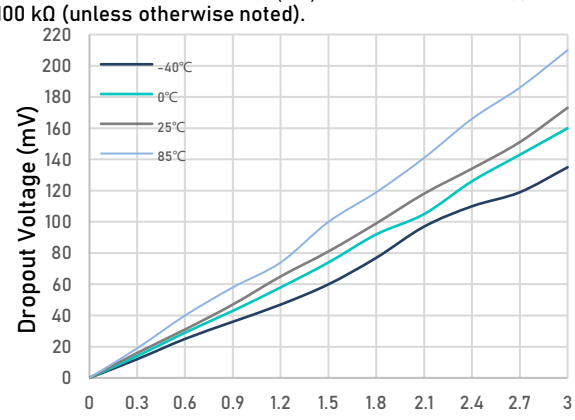
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



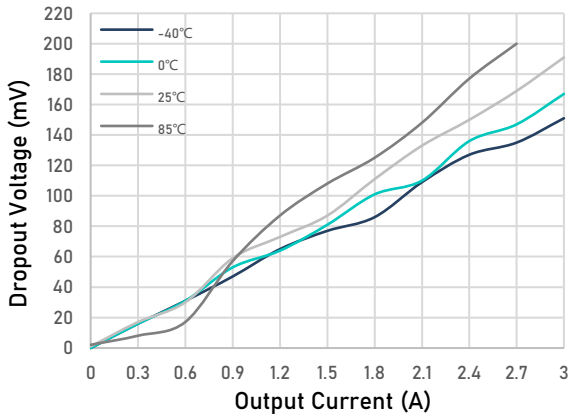
V_{IN} = 1.2 V, V_{BIAS} = 5.0 V, slew rate = 1 A/µs, $C_{NR/SS}$ = C_{FF} = 10 nF, C_{OUT} = 47 µF || 10 µF || 10 µF

Fig19. Load Transient vs Time and DC Load (V_{OUT} = 0.9 V)



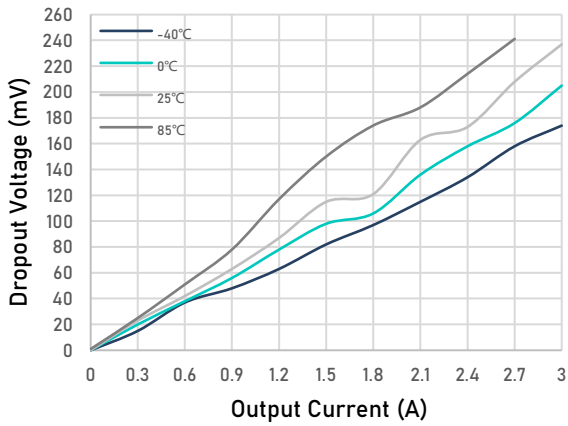
V_{IN} = 1.4 V, V_{BIAS} = 0 V

Fig20. Dropout Voltage vs Output Current Without Bias



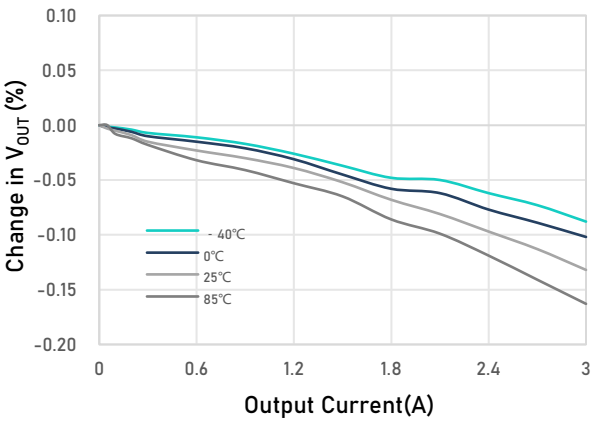
V_{OUT} = 3.95 V

Fig21. Dropout Voltage vs Output Voltage



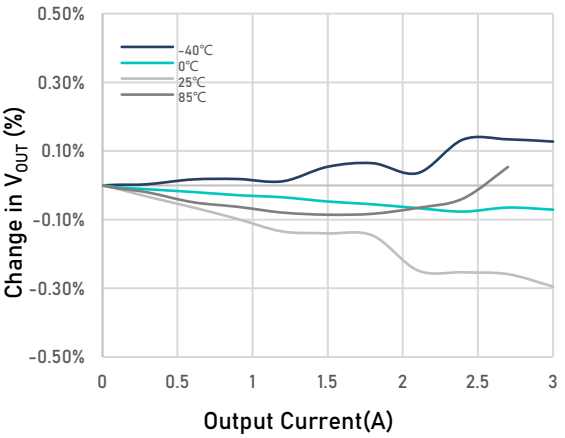
V_{OUT} = 5 V

Fig22. Dropout Voltage vs Output Voltage



V_{IN} = 1.4 V , V_{BIAS} = 0 V

Fig23. Load Regulation Without Bias

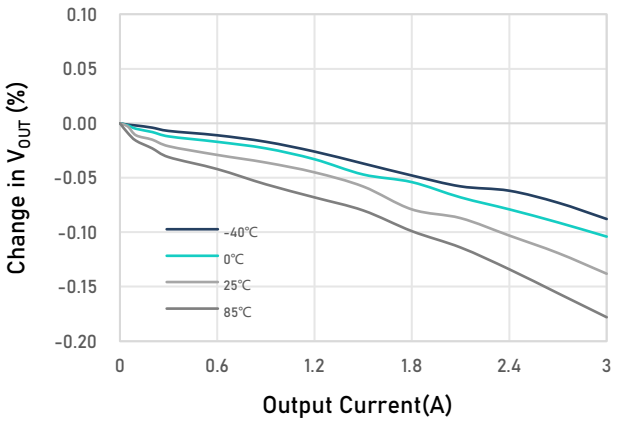


V_{IN} = 4.45 V

Fig24. Load Regulation (3.95 V Output)

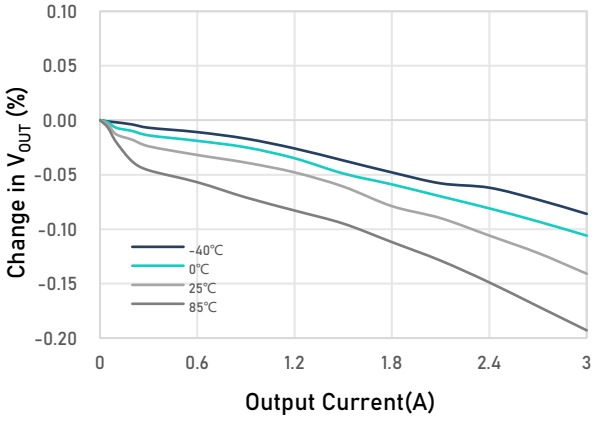
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



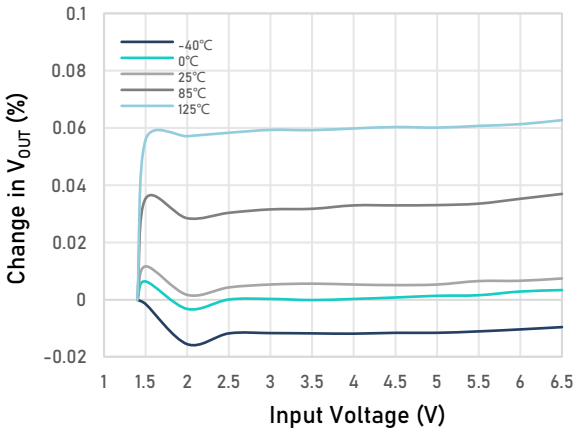
V_{IN} = 3.8 V

Fig.25 Load Regulation vs I_{OUT} (3.3 V Output)



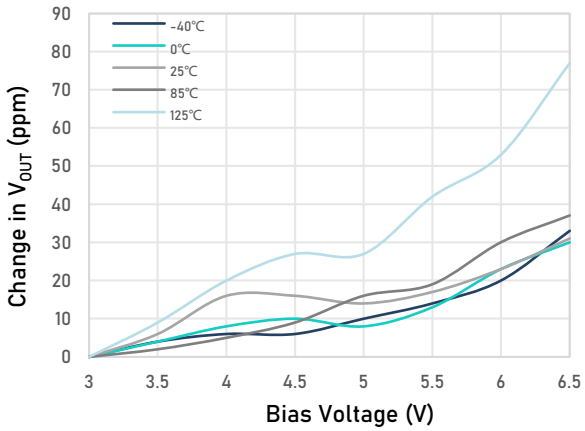
V_{IN} = 5.5 V

Fig.26 Load Regulation vs I_{OUT} (5 V Output)



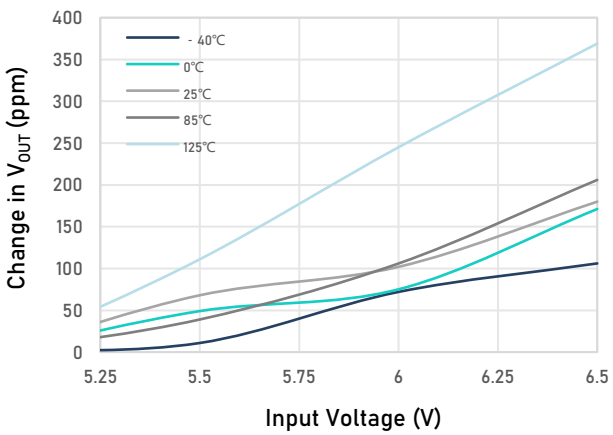
V_{OUT} = 0.8 V, I_{OUT} = 5 mA

Fig.27 Line Regulation vs V_{IN}



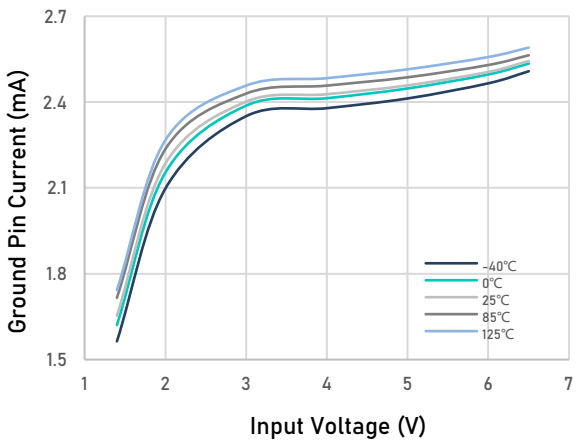
V_{OUT} = 0.8 V, V_{IN} = 1.1 V, I_{OUT} = 5 mA, V_{BIAS} = 5 V

Fig.28 Line Regulation With Bias



I_{OUT} = 5 mA

Fig.29 Line Regulation vs Input Voltage (5 V Output)

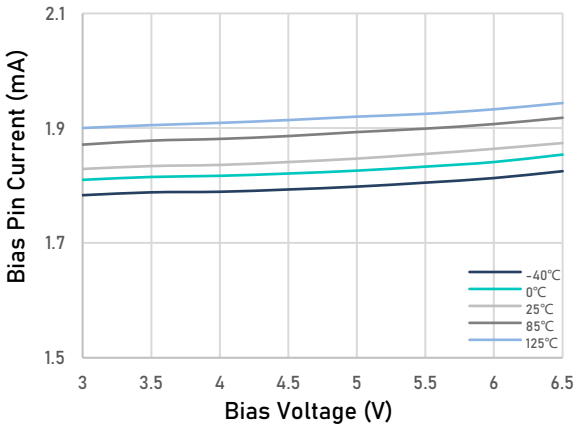


V_{BIAS} = 0 V , I_{OUT} = 0 mA

Fig30. Quiescent Current vs Input Voltage

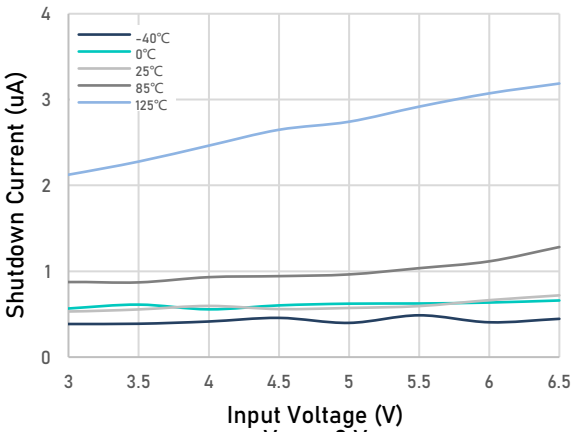
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



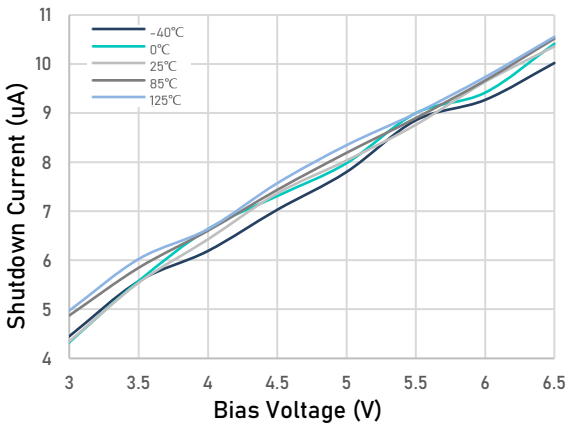
V_{IN} = 1.1 V , I_{OUT} = 5 mA

Fig31. Quiescent Current vs Bias Voltage



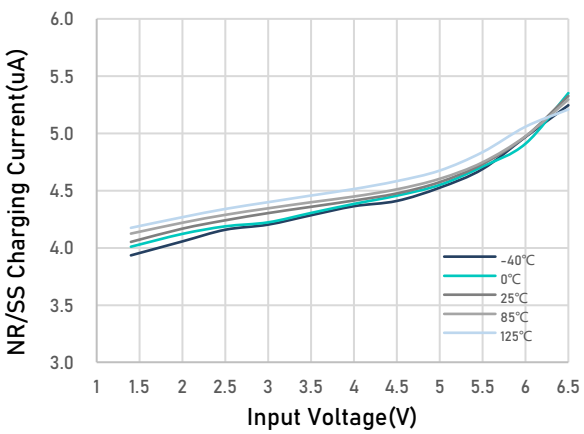
V_{BIAS} = 0 V

Fig32. Shutdown Current vs Input Voltage



V_{IN} = 1.1 V

Fig33. Shutdown Current vs Bias Voltage



V_{BIAS} = 0 V

Fig34. $I_{NR/SS}$ Current vs Input Voltage

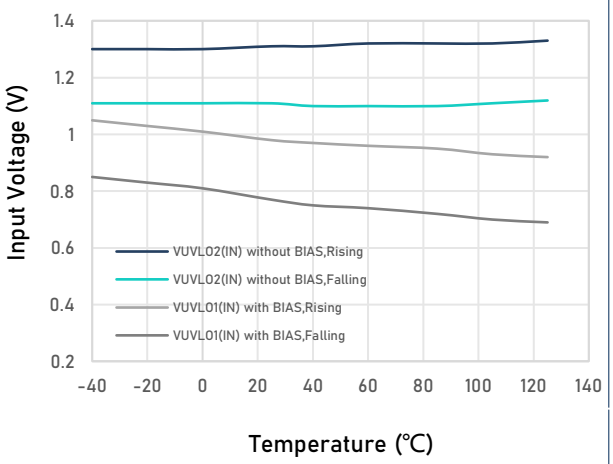
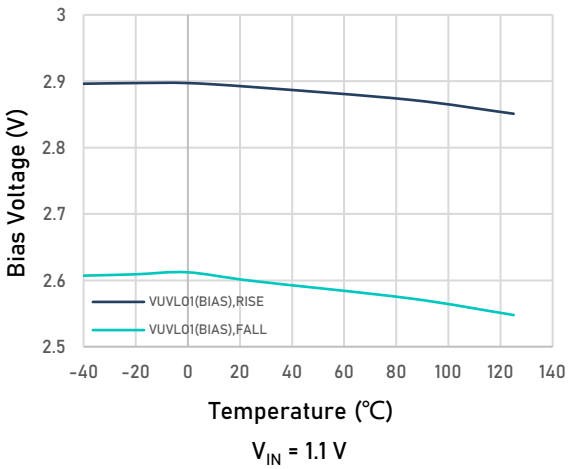


Fig35. V_{IN} UVLO vs Temperature

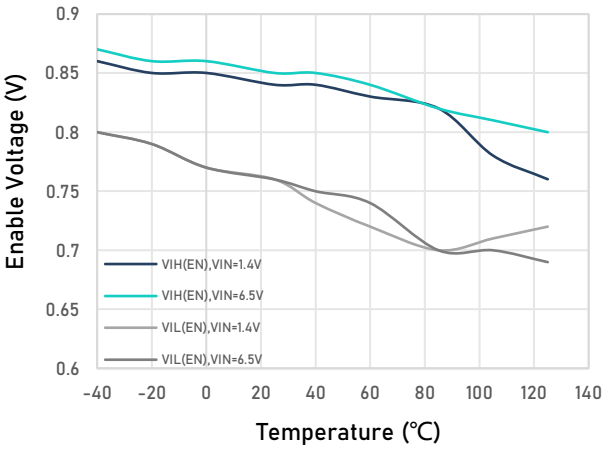


V_{IN} = 1.1 V

Fig36. V_{BIAS} UVLO vs Temperature

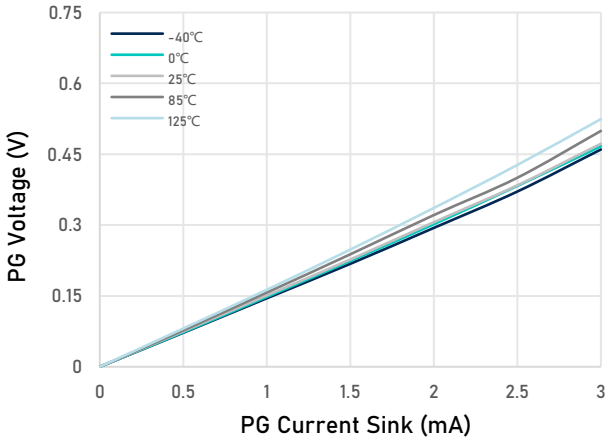
Typical Performance Characteristics

Note: at T_A = 25°C, V_{IN} = 1.4 V or V_{IN} = $V_{OUT(NOM)}$ + 0.4 V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted).



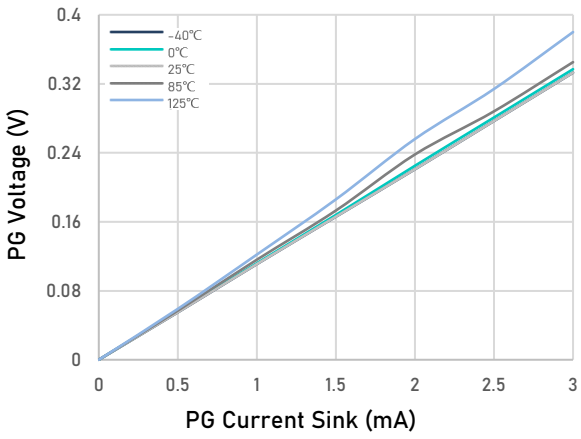
V_{IN} = 1.4 V , 6.5 V

Fig37. Enable Threshold vs Temperature



V_{IN} = 1.4 V

Fig38. PG Voltage vs PG Current Sink



V_{IN} = 6.5 V

Fig39. PG Voltage vs PG Current Sink

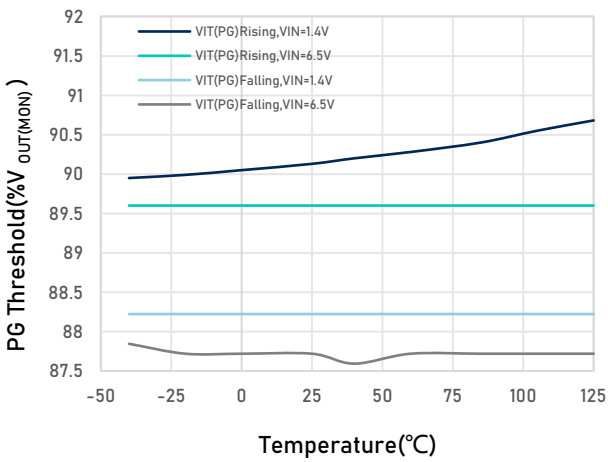


Fig40. PG Threshold vs Temperature

Applications Information

General

The LTP7693 is a linear voltage regulator with an input range of 1.1 V to 6.5 V and an output voltage range of 0.8 V to 5.15 V with a 1% accuracy and a 3 A maximum output current. The LTP7693 has an integrated charge pump for ease of use and an external bias rail to allow for the lowest dropout across the entire output voltage range.

Recommended Capacitor Types

The LTP7693 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (that is, V_{IN} = 5.5 V to V_{OUT} = 5.15 V) the derating can be greater than 50% and must be taken into consideration.

Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The LTP7693 is designed and characterized for operation with ceramic capacitors of 47 µF or greater (22 µF or greater of capacitance) at the output and 10 µF or greater (5 µF or greater of capacitance) at the input. Using at least a 47 µF capacitor is highly recommended at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. If the trace inductance from the input supply to the LTP7693 is high, a fast current transient can cause VIN to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen the ringing and to keep it below the device absolute maximum ratings.

A combination of multiple output capacitors boosts the high-frequency PSRR, as illustrated in several of the PSRR curves. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating in conjunction with the PSRR boost circuit optimizes PSRR for the frequency range of 400 kHz to 700 kHz, a typical range for dc-dc supply switching frequency. This 47-µF || 10-µF || 10-µF combination also ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 80% at 5.0 V, so the addition of the two 10-µF capacitors ensures that the capacitance is at or above 22 µF.

Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The LTP7693 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$).The use of an external $C_{NR/SS}$ is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, the LTP7693 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Soft-start ramp time can be calculated with Equation 1:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (1)$$

Note that $I_{NR/SS}$ is provided in the Electrical Characteristics table and has a typical value of 6.6 µA.

Applications Information

Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10 nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled. For a detailed description, see the Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator application report.

Soft-Start and In-Rush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

In-rush current is defined as the current into the LDO at the IN pin during start-up. In-rush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 2:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \qquad (2)$$

where:

- $V_{OUT(t)}$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT(t)}$ / dt is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

Optimizing Noise and PSRR

The ultra-low noise floor and PSRR of the device can be improved by careful selection of:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the mid-band frequency range
- C_{OUT} for the high-frequency range
- V_{IN} – V_{OUT} for all frequencies, and
- V_{BIAS} at lower input voltages

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. The feed-forward capacitor can be optimized to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth, thus improving mid-band PSRR. Larger output capacitors and various output capacitors can be used to improve high-frequency PSRR.

A higher input voltage improves the PSRR by giving the device more headroom to respond to noise on the input; see the PSRR vs Frequency and V_{IN} With Bias curve. A bias rail also improves the PSRR at lower input voltages because greater headroom is provided for the internal circuits.

The noise-reduction capacitor filters out low-frequency noise from the reference and the feed-forward capacitor reduces output voltage noise by filtering out the mid-band frequency noise. However, a large feed-forward capacitor can create some new issues that are discussed in the Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator application report.

A large output capacitor reduces high-frequency output voltage noise. Additionally, a bias rail or higher input voltage improves the noise because greater headroom is provided for the internal circuits.

Table 1 lists the output voltage noise for the 10Hz to 100kHz band at a 5.15 V output for a variety of conditions with an input voltage of 5.4 V, an R1 of 6.05 kΩ, and a load current of 3 A. The 5.15 V output is chosen because this output is the worst-case condition for output voltage noise.

Applications Information

Table 1. Output Noise Voltage at a 5.0 V Output

Output Voltage Noise (µVRMS)	$C_{NR/SS}$ (nF)	C_{FF} (nF)	C_{OUT} (µF)
11	10	10	47 || 10 || 10
8.6	100	10	47 || 10 || 10
7.6	100	100	47 || 10 || 10
8.5	100	10	1000
7	100	100	1000

Charge Pump Noise

The device internal charge pump generates a minimal amount of noise.

Using a bias rail minimizes the internal charge pump noise when the internal voltage is clamped, thereby reducing the overall output noise floor.

The high-frequency components of the output voltage noise density curve are filtered out in most applications by using 10-nF to 100-nF bypass capacitors close to the load. Using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution.

ANY-OUT Programmable Output Voltage

The LTP7693 can use either external resistors or the internally-matched ANY-OUT feedback resistor network to set output voltage. The ANY-OUT resistors are accessible via pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin is can be connected to ground (active) or left open (floating), or connected to

SNS. ANY-OUT programming is set by Equation 3 as the sum of the internal reference voltage ($V_{NR/SS}$ = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50mV (pin 5), 100mV (pin 6), 200mV (pin 7), 400mV (pin 9), 800mV (pin 10), or 1.6V (pin 11). By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{FB}.

$$V_{OUT} = V_{NR/SS} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (3)$$

The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8 V to 3.95 V in 50-mV steps when tying these pins to ground. There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. As with the adjustable

operation, the output voltage is set according to Equation 4 except that R1 and R2 are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal

feedback network by lowering the value of R1. See the Increasing ANY-OUT Resolution for LILO Conditions section for additional information.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (4)$$

Applications Information

ANY-OUT Operation

Considering the use of the ANY-OUT internal network (where the unit resistance of 1R is equal to 6.05 kΩ) the output voltage is set by grounding the appropriate control pins, as shown in Figure . When grounded,

all control pins add a specific voltage on top of the internal reference voltage (VNR/SS = 0.8 V). The output voltage can be calculated by Equation 6 and Equation 7. Figure 41 and Figure 42 show a 0.9 V output voltage, respectively, that provide an example of the circuit usage with and without bias voltage.

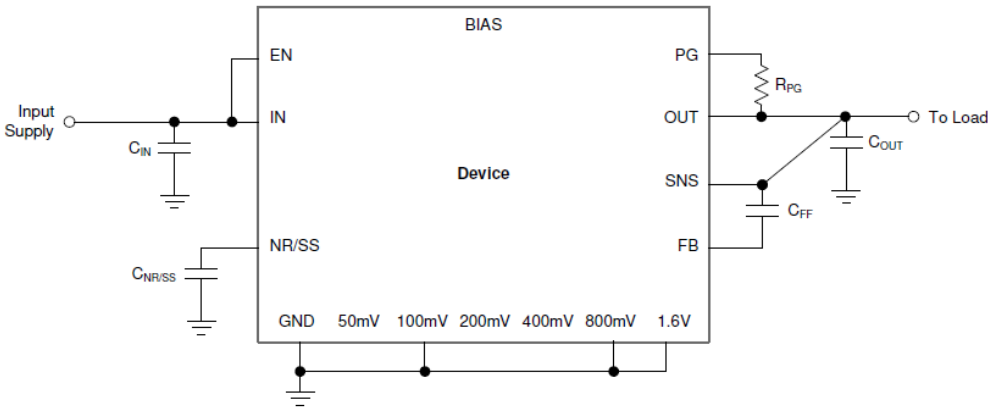


Figure 41. ANY-OUT Configuration Circuit (3.3-V Output, No External Bias)

$V_{OUT(nom)} = V_{NR/SS} + 1.6\ V + 0.8\ V + 0.1\ V = 0.8\ V + 1.6\ V + 0.8\ V + 0.1\ V = 3.3\ V$

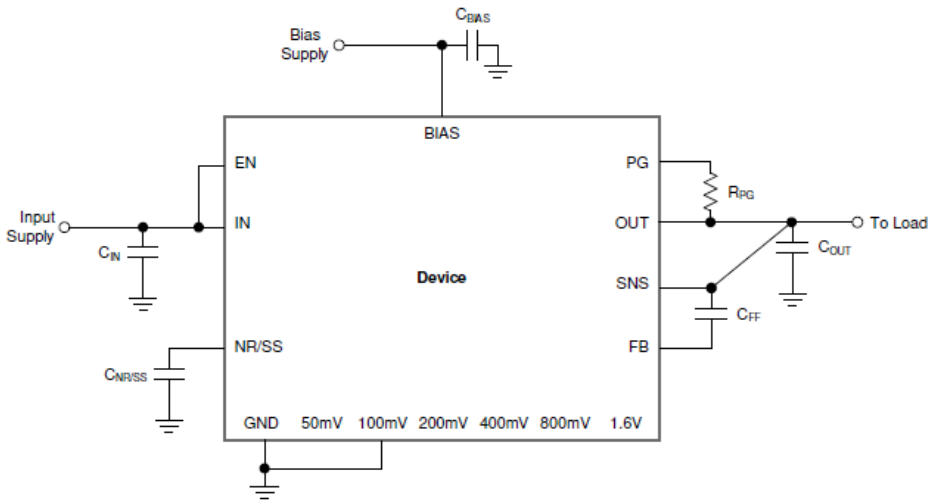


Figure 42. ANY-OUT Configuration Circuit (0.9-V Output with Bias)

VOUT(nom) = VNR/SS + 0.1 V = 0.8 V + 0.1 V = 0.9 V

Increasing ANY-OUT Resolution for LILO Conditions

As with the adjustable operation, the output voltage is set according to Equation 5, except that R1 and R2 are internally integrated and matched for higher accuracy. Tying any of the ANY-OUT pins to SNS can increase the resolution of the internal feedback network by lowering the value of R1. One of the more useful pin combinations is to tie the 800mV pin to SNS, which reduces the resolution by 50% to 25 mV but limits the range.

Applications Information

ANY-OUT Operation

25 mV but limits the range. The new ANY-OUT ranges are 0.8 V to 1.175 V and 1.6 V to 1.975 V.

Current Sharing

Current sharing is possible through the use of external operational amplifiers. For more details, see the 6A Current-Sharing Dual LDO design guide.

Adjustable Operation

The LTP7693 can be used either with the internal ANY-OUT network or by using external resistors. Using the ANY-OUT network allows the LTP7693 to be programmed from 0.8 V to 3.95 V. To extend this output voltage range to 5.15 V, external resistors must be used. This configuration is referred to as the adjustable configuration of the LTP7693 throughout this document. Regardless whether the internal resistor network or whether external resistors are used, the output voltage is set by two resistors, as shown in Figure 43. Using the internal resistor ensures a 1% accuracy and minimizes the number of external components.

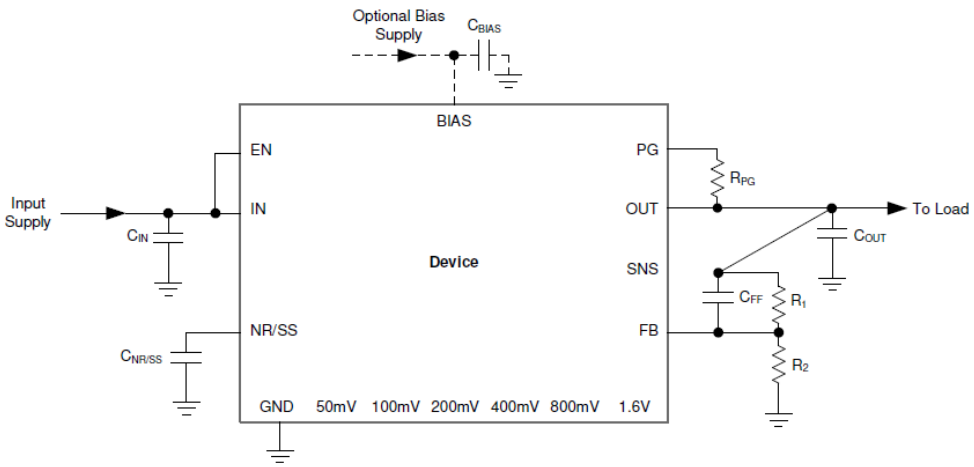


Figure 43. Adjustable Operation

R1 and R2 can be calculated for any output voltage range using Equation 8. This resistive network must provide a current equal to or greater than 5 µA for dc accuracy. Using an R1 of 6.05 kΩ is recommended to optimize the noise and PSRR.

Sequencing Requirements

Supply and enable sequencing is only required when the bias rail is present. The start-up is always monotonic, independent of the sequencing requirements. Under these conditions the following requirements apply:

V_{BIAS} and V_{IN} can be sequenced in any order, as long as V_{EN} is tied to V_{IN} or established after VIN, as shown in Figure 44.

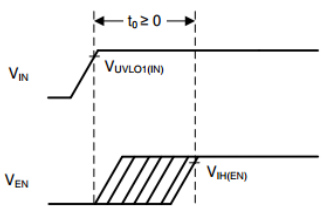


Figure 44. Sequencing Diagram

Applications Information

Two typical application circuits for implementing the sequencing requirements are detailed in the Sequencing with a Power-Good DC-DC Converter Pin and Sequencing with a Microcontroller (MCU) sections

Sequencing with a Power-Good DC-DC Converter Pin

When a dc-dc converter is used to power the device and the PG of the dc-dc converter is used to enable the device, pull PG up to V_{IN}, as shown in Figure 45.

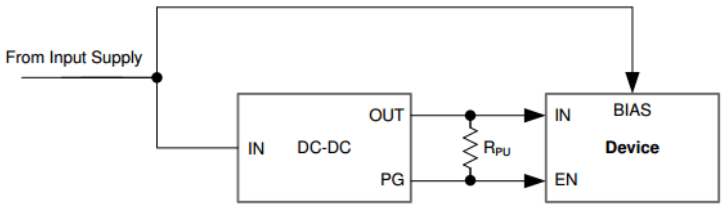


Figure 45. Sequencing with a DC-DC Converter and PG

Sequencing with a Microcontroller (MCU)

If a push-pull output stage is used to provide the enable signal to the device and the enable signal can possibly come before V_{IN} when a bias is present (such as with an MCU), convert the enable signal to an open-drain signal as shown in Figure 46. Using an open-drain signal ensures that if the signal arrives before V_{IN}, then the enable voltage does not violate the sequencing requirement.

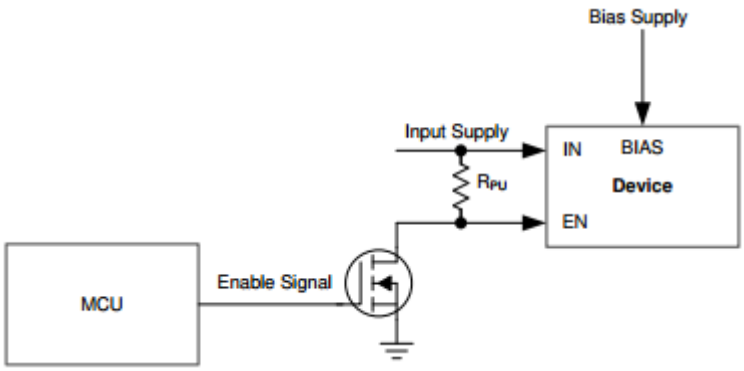


Figure 46. Push-Pull Enable to Open-Drain Enable

Power-Good Operation

To ensure proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level.

Using a large CFF with a small CNR/SS causes the power-good signal to incorrectly indicate that the output voltage has settled during turn-on. The CFF time constant must be greater than the soft-start time constant to ensure proper operation of the PG during start-up.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

Applications Information

Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device shuts down when the input supply or bias supply collapse.

The UVLO circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the UVLO to assert for a short time; however, the UVLO circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuit does not fully discharge, the internal circuits of the output are not fully disabled.

The effect of the downward line transient can be mitigated by either using a larger input capacitor to limit the fall time of the input supply when operating near the minimum VIN, or by using a bias rail.

Figure 47 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

·Region A: The device does not turn on until the input reaches the UVLO rising threshold.

·Region B: Normal operation with a regulated output

·Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device is still enabled.

·Region D: Normal operation with a regulated output

·Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up then follows.

·Region F: Normal operation followed by the input falling to the UVLO falling threshold.

·Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

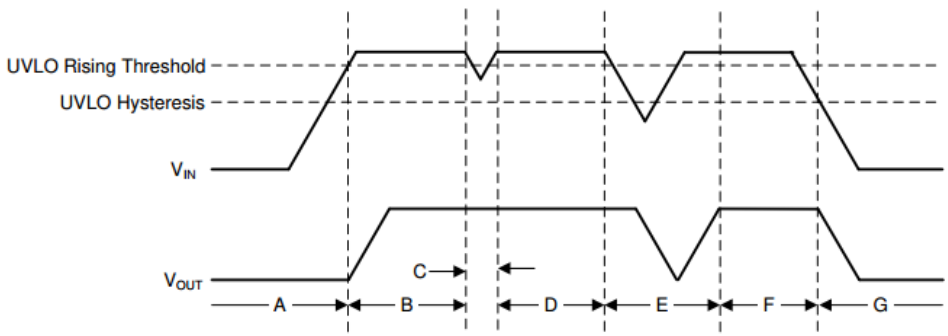


Figure 47. Typical UVLO Operation

Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage (V_{DO} = V_{IN} – V_{OUT}) that is required for regulation. When V_{IN} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch;

Dropout voltage is affected by the drive strength for the gate of the pass element, which is nonlinear with respect to V_{IN} on this device because of the internal charge pump. The charge pump causes a higher dropout voltage at lower input voltages when a bias rail is not used, as illustrated in the Dropout Voltage vs Input Voltage Without Bias curve.

For this device, dropout voltage increases exponentially when the input voltage nears its maximum operating voltage because the charge pump is internally clamped to 8.0 V;

Applications Information

Behavior when Transitioning from Dropout into Regulation

Some applications may have transients that place the device into dropout, especially because this device is a high-current linear regulator. A typical application with these conditions requires setting $V_{IN} \leq V_{DO}$ in order to keep the device junction temperature within its specified operating range. A load transient or line transient in these conditions can place the device into dropout, such as a load transient from 1 A to 4 A at 1A/µs when operating with a VIN of 5.4 V and a V_{OUT} of 5.0 V.

The load transient saturates the error amplifier output stage when the pass element is fully driven on, thus making the pass element function like a resistor from VIN to VOUT. The error amplifier response time to this load transient (I_{OUT} = 4 A to 1 A at 1 A/µs) is limited because the error amplifier must first recover from saturation and then place the pass element back into active mode. During the recovery from the load transient, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}. If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot because these solutions provide a path to dissipate the excess charge.

Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained; see the Load Transient vs Time and V_{OUT} With Bias curve. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 48 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state.

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B).
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C).

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F).
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G).

Transitions between current levels changes the internal power dissipation because the LTP7693 is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This different output voltage level shows up in the various load transient responses; see the Load Transient vs Time and VOUT With Bias curve.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor; see the Load Transient vs Time and Slew Rate curve.

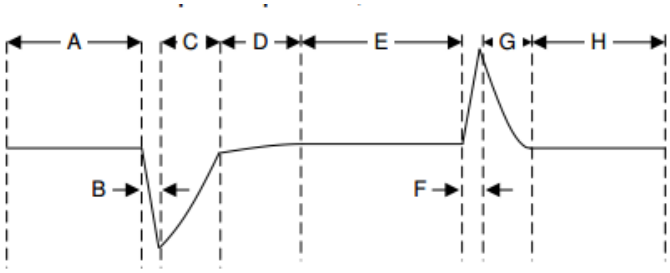


Figure 48. Load Transient Waveform

Applications Information

Negatively-Biased Output

The device does not start or operate as expected if the output voltage is pulled below ground. This issue commonly occurs when powering a split-rail system where the negative rail is established before the device is enabled. Several application solutions are:

- Enable the device before the negative regulator and disable the device after the negative regulator.
- Delaying the EN voltage with respect to the IN voltage allows the internal pulldown resistor to discharge any voltage at OUT. If the discharge circuit is not strong enough to keep the output voltage at ground, then use an external pulldown resistor.
- Place a zener diode from IN to OUT to provide a small positive dc bias on the output when the input is supplied to the device, as shown in Figure 49.

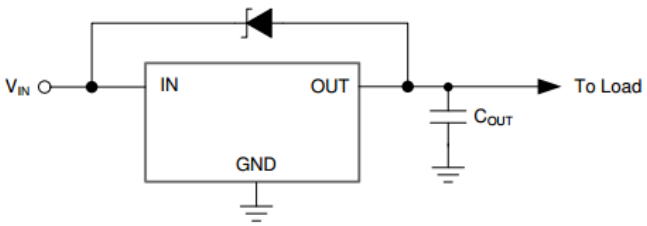


Figure 49. Zener Diode Placed from IN to OUT

- Use a PFET to isolate the output of the device from the load causing the negative bias when the device is off, as shown in Figure 50.

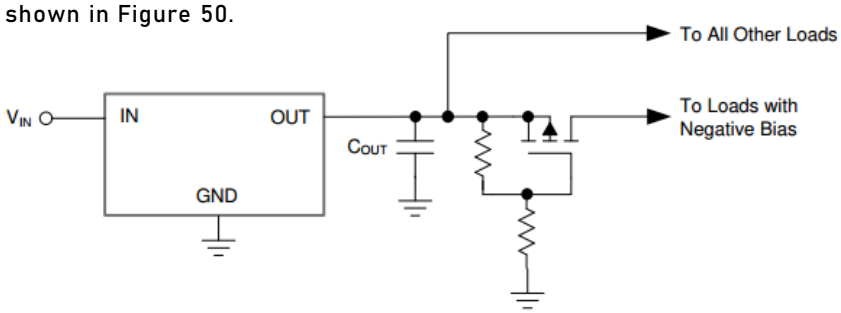


Figure 50. PFET to Isolate the Output from the Load

Reverse Current Protection

As with most LDOs, this device can be damaged by excessive reverse current.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT}, then the input supply collapses quickly and the load current becomes very small
- The output is biased when the input supply is not established
- The output is biased above the input supply

If an excessive reverse current flow is expected in the application, then external protection must be used to protect the device. Figure 51 shows one approach of protecting the device.

Applications Information

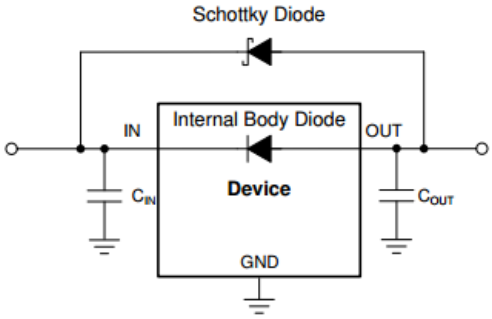


Figure 51. Example Circuit for Reverse Current Protection Using a Schottky Diode

Power Dissipation (PD)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be calculated using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the LTP7693 allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (TJ) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 6. The equation is rearranged for output current in Equation 7.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (6)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (7)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the Electrical Characteristics table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance ($R_{\theta JCbo}$t) plus the thermal resistance contribution by the PCB copper.

Applications Information

Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the Electrical Characteristics table and are used in accordance with Equation 8.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (8)$$

where:

- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

Recommended Area for Continuous Operation (RACO)

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator can be separated into the following parts, and is shown in Figure 52:

- Limited by dropout: Dropout voltage limits the minimum differential voltage between the input and the output (V_{IN} – V_{OUT}) at a given output current level.
- Limited by rated output current: The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- Limited by thermals: The shape of the slope is given by Equation 11. The slope is nonlinear because the junction temperature of the LDO is controlled by the power dissipation across the LDO; therefore, when V_{IN}

–V_{OUT} increases, the output current must decrease in order to ensure that the rated junction temperature of the device is not exceeded. Exceeding this rating can cause the device to fall out of specifications and reduces long-term reliability.

- Limited by V_{IN} range: The rated input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

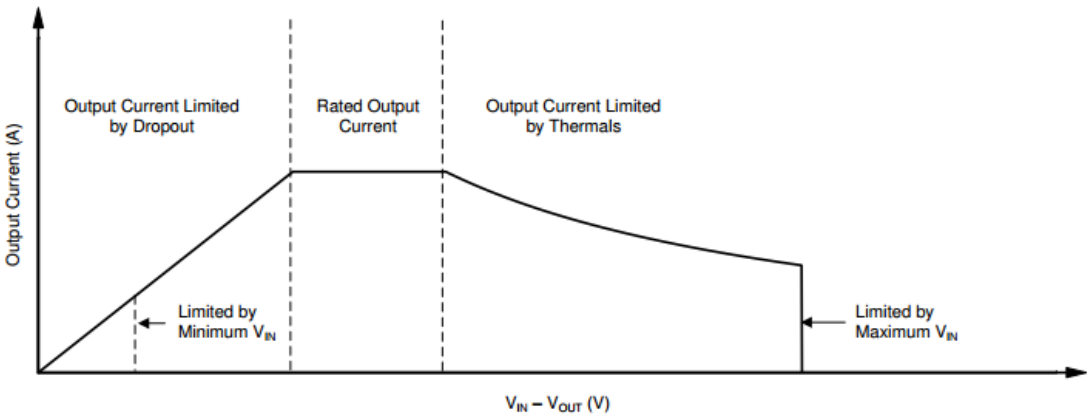
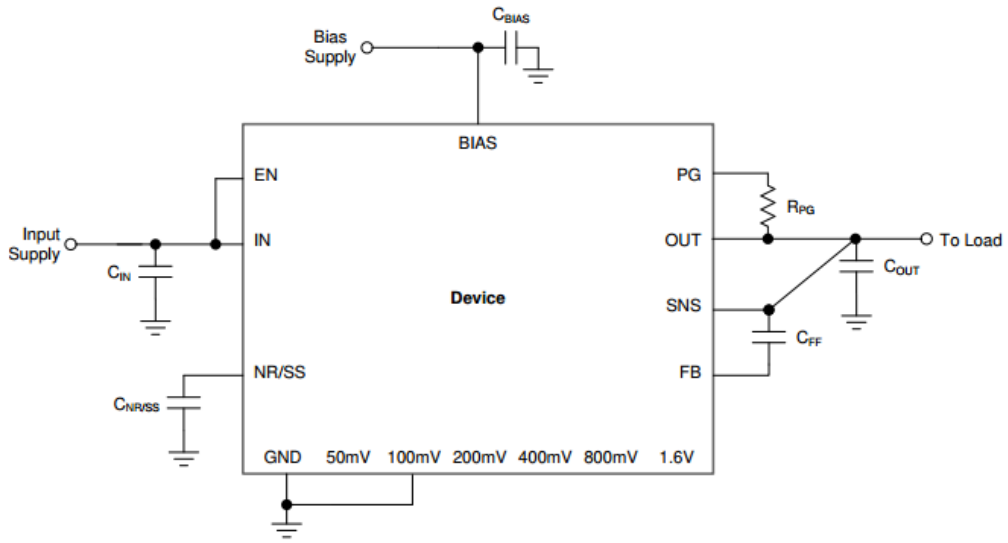
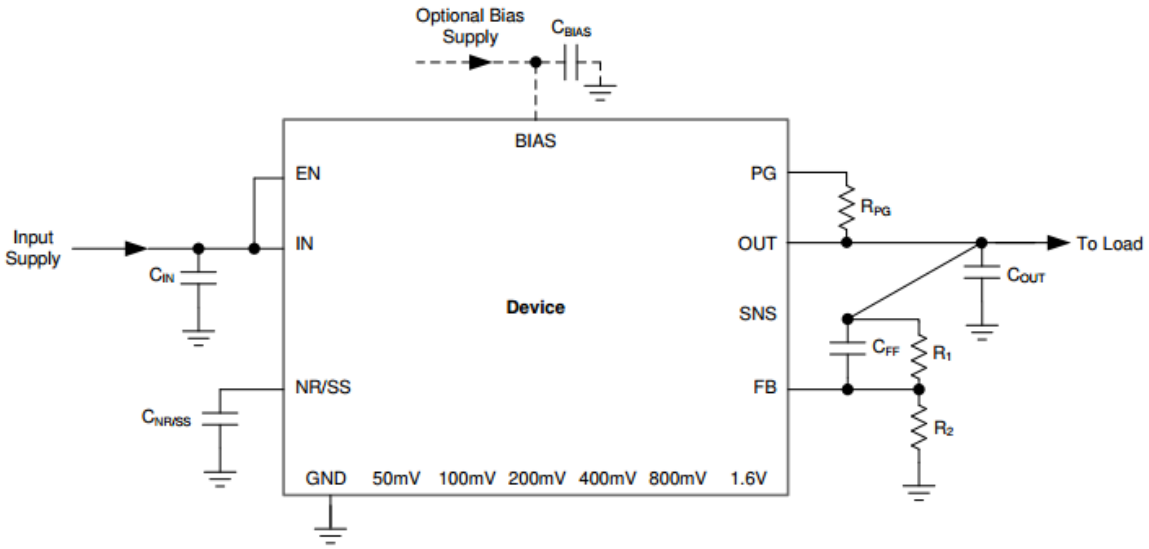


Figure 52. Continuous Operation Slope Region Description

Application Circuits



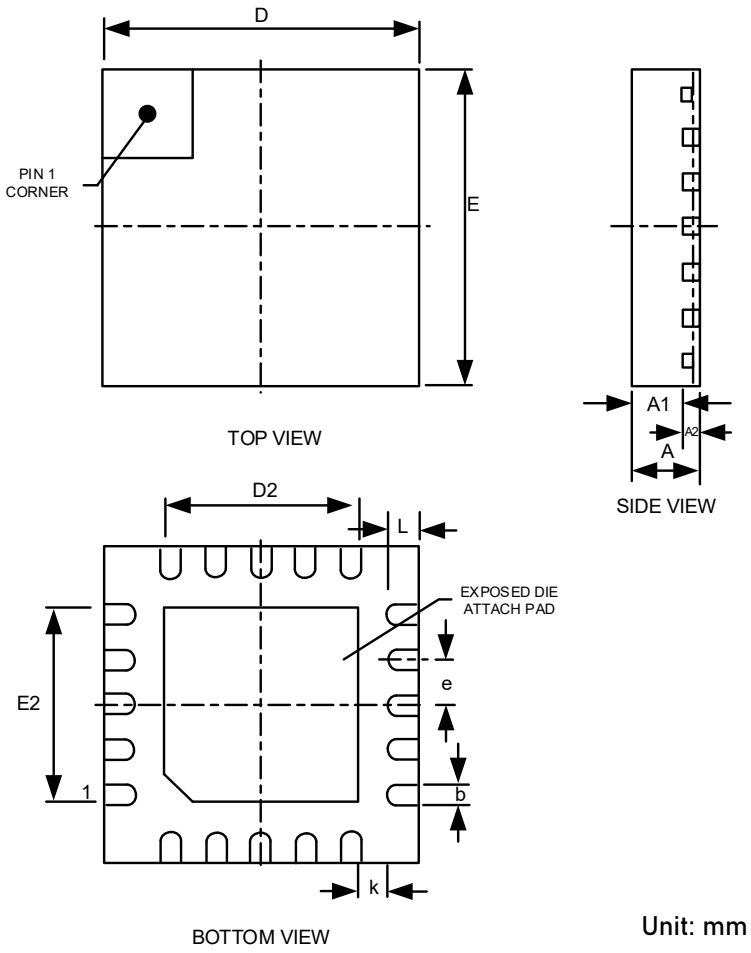
Low-Input, Low-Output (LILO) Voltage Conditions



Typical Application for a 5.0 V Rail

Package Dimension

QFN3.5×3.5-20



Unit: mm

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1		0.550	
A2		0.203REF	
b	0.180	0.230	0.280
D		3.5BSC	
E		3.5BSC	
e		0.5BSC	
D2	2.050	2.150	2.250
E2	2.050	2.150	2.250
L	0.250	0.350	0.450
K		0.325REF	