1. General Description

The LTD211X family are high-precision, low-power, 16-bit analog-to-digital converters in a small-sized VSSOP-10L package. Oscillator and low-drift voltage reference are integrated internally. LTD2113 and LTD2114 support two single-ended input (or one differential input), while LTD2115 and LTD2118 support up to four single-ended inputs (or two differential inputs), switched by an input multiplexer. LTD2114 and LTD2115 provide a comparator feature for under-voltage and over-voltage detection. LTD2118 provides a precise internal temperature sensor for real-time temperature monitoring.

The LTD211X family supports a conversion rate up to 1024 samples per second (SPS). The integrated programmable gain amplifier (PGA) can modulate the input range from ±256 mV to ±6.144 V, to be suitable for both large and small input analog signals (LTD2113 excluded, fixed at ± 2.048 V). LTD2113, LTD2114 and LTD2115 is I^2C compatible with four pin-selectable addresses. LTD2118 is SPI compatible.

The LTD211X family performs conversion in either continuous-mode or single-shot mode. The typical supply current value in continuous operation is 150 μA. In single-shot mode, the device enters power-down status automatically after the conversion is completed, which significantly suppresses the power consumption during idling. Such features make the LTD211X family appropriate for power sensitive applications such as battery-powered devices.

The LTD211X family are available in 3 mm × 3 mm VSSOP-10L packages and specified in temperature range from -40℃ to 125℃.

2. Features and Benefits

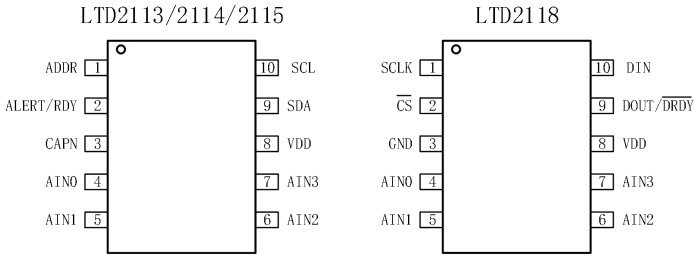
- Wide voltage supply: 2 V to 5 V
- Low current consumption: 150 μA in continuous operation
- Wide Data rate option: 8 SPS to 1024 SPS
- Single-cycle settling
- Integrated voltage reference
- Integrated oscillator
- I^2C compatible: four pin-selectable addresses (LTD2113, LTD2114 and LTD2115)
- SPI compatible (LTD2118 only)
- Four single-ended or two differential inputs (LTD2115 and LTD2118)
- Integrated comparator (LTD2114 and LTD2115)
- Integrated temperature sensor (LTD2118 only)
- Operating temperature range: -40℃ to 125℃
- Small package: 3 mm × 3 mm VSSOP-10L

3. Applications

- Temperature measurement system
- Portable instruments

- Battery voltage and current monitoring
- Factory automation and process control
- Consumer electronics

4. Pin Configuration (Top View)



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5. Revision History

Version 0

Initial version.

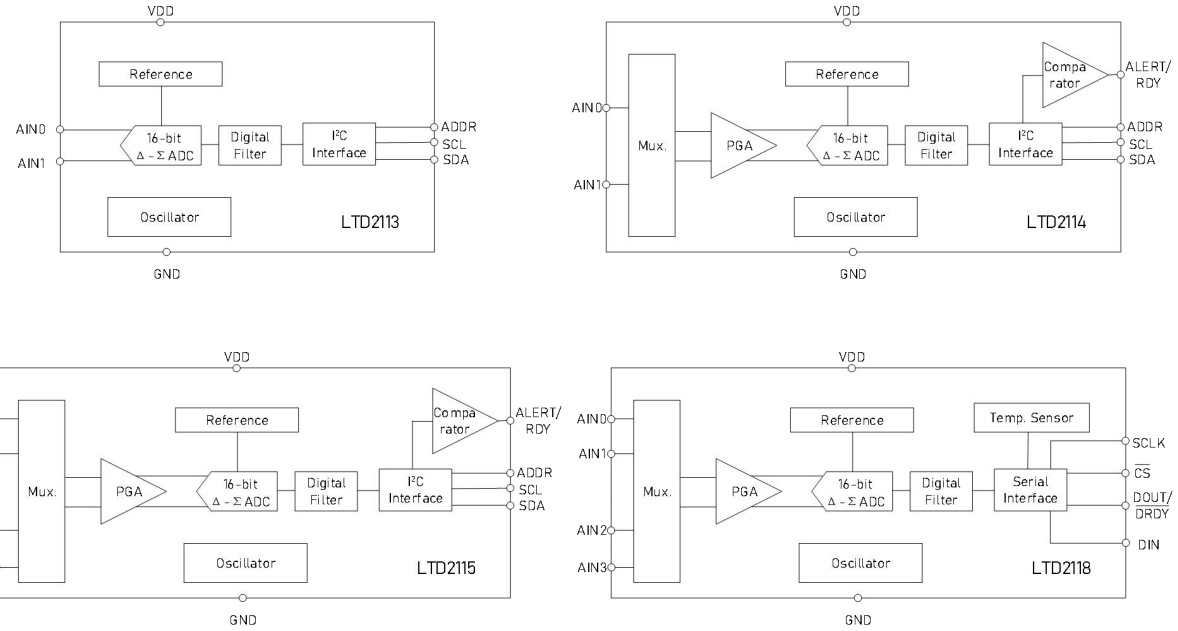
6. Device Comparison

Part Number	Input Channels		PGA	Comparator	Temperature Sensor	Interface
	Single-ended	Differential				
LTD2113	2	1	NA	NA	NA	I²C
LTD2114	2	1	Integrated	Integrated	NA	I²C
LTD2115	4	2	Integrated	Integrated	NA	I²C
LTD2118	4	2	Integrated	NA	Integrated	SPI

7. Pin Description

Pin Name	Pin Number				Description
	LTD211 3	LTD211 4	LTD211 5	LTD211 8	
ADDR	1	1	1	NA	I²C slave address select
SCLK	NA	NA	NA	1	Serial clock input
ALERT/RDY	NA	2	2	NA	Comparator output or conversion ready (LTD2114 and LTD2115 only)
$\overline{CS}$	NA	NA	NA	2	Chip select, active low. Connect to GND if not used.
GND	3	3	3	3	Ground
AIN0	4	4	4	4	Analog input 0
AIN1	5	5	5	5	Analog input 1
AIN2	NA	NA	6	6	Analog input 2
AIN3	NA	NA	7	7	Analog input 3
VDD	8	8	8	8	Power supply. Connect a 0.1-µF decoupling capacitor to GND.
SDA	9	9	9	NA	Serial data. Transmits and receives data
DOUT/$\overline{DRDY}$	NA	NA	NA	9	Serial data output combined with data ready indicator, active low
SCL	10	10	10	NA	Serial clock input, locks data on SDA
DIN	NA	NA	NA	10	Serial data input

8. Functional Block Diagram



9. Ordering Information

Part Number	Package Type	Quantity	Mark Code
LTD2113XV10/R8	VSSOP-10L	Tape and Reel, 4000	D2113
LTD2114XV10/R8	VSSOP-10L	Tape and Reel, 4000	D2114
LTD2115XV10/R8	VSSOP-10L	Tape and Reel, 4000	D2115
LTD2118XV10/R8	VSSOP-10L	Tape and Reel, 4000	D2118

10. Specifications

10.1. Limiting Value

Parameter	MIN	MAX	UNIT
Power supply voltage, VDD to GND	-0.3	7	V
Analog input voltage, AIN0, AIN1, AIN2, AIN3	GND-0.3	VDD+0.3	V
Digital input voltage, SDA, SCL, ADDR, ALERT/RDY	GND-0.3	5.5	V
Digital input voltage, DIN, DOUT/$\overline{DRDY}$, SCLK, $\overline{CS}$	GND-0.3	VDD+0.3	V
Input current continuous, any pin except supply pins	-10	10	mA
Operating ambient T_A	-40	125	℃
T_{STG}	-60	150	℃

10.2. ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

10.3. Recommended Operating Conditions

Parameter		Conditions	Min	Nom	Max	Unit
Power Supply						
	Power supply	VDD to GND	2		5.5	V
Analog Inputs						
FSR	Full-scale analog input range	$V_{IN} = V_{AINP} - V_{AINN}$	±0.256		±6.144	V
V_{AINX}	Absolute input voltage		GND		VDD	V
Digital Inputs						
	Input voltage	LTD2113, LTD2114, LTD2115	GND		5.5	V
	Input voltage	LTD2118	GND		VDD	V
Temperature						
T_A	Ambient temperature		-45		125	℃

10.4. Characteristics for LTD2113, LTD2114 and LTD2115

Minimum and maximum specifications are measured from T_A = –40°C to +125°C; typical specifications are measured at T_A = 25°C; all specifications are measured at VDD = 3.3 V, AVSS = 0 V, data rate = 8 SPS, FSR = 2.048 V (unless otherwise noted).

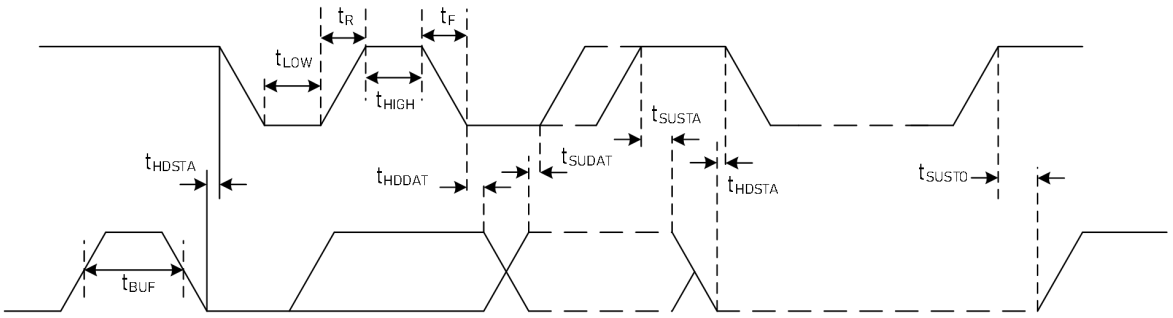
Parameter	Conditions	Min	Typ	Max	Unit
Analog Inputs					
Common-mode input impedance	FSR = ±6.144 V		10		MΩ
	FSR = ±4.096 V, FSR = ±2.048 V		6		
	FSR = ±1.024 V		3		
	FSR = ±0.512 V, FSR = ±0.256 V		100		
Differential input impedance	FSR = ±6.144 V		22		MΩ
	FSR = ±4.096 V		15		
	FSR = ±2.048 V		4.9		
	FSR = ±1.024 V		2.4		
	FSR = ±0.512 V, FSR = ±0.256 V		0.71		

Performance						
	Resolution	No missing code	16			Bits
DR	Data rate		8, 16, 32, 64, 128, 256, 512, 1024			SPS
	Data rate variation		-10%		+10%	
INL	Integral non-linearity	DR = 8 SPS, FSR = ±2.048 V			1	LSB
	Offset error	FSR = ±2.048 V, differential inputs	-3	±1	3	LSB
		FSR = ±2.048 V, single-ended inputs		±3		
	Offset drift	FSR = ±2.048 V, T_A = -40 to 125 ℃		0.005		LSB/℃
	Offset long-term drift	FSR = ±2.048 V, T_A = 125 ℃, 1000 hrs		±1		LSB
	Offset power supply rejection	FSR = ±2.048 V, DC supply variation		1		LSB/V
	Offset channel match	Match between any two inputs		3		LSB
	Gain effor	FSR = ±2.048 V, T_A = 25 ℃		0.01%	0.15%	
	Gain drift	FSR = ±0.256 V		7		ppm/℃
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V		5		
	Gain match	Match between any two gains		0.02%	0.1%	
	Gain channel match	Match between any two inputs		0.05%	0.1%	
	Gain long-term drift	FSR = ±2.048 V, T_A = 125 ℃, 1000 hrs		±0.05%		
CMRR	Common-mode rejection ratio	DC, FSR = ±0.256 V		105		dB
		DC, FSR = ±2.048 V		100		
		DC, FSR = ±6.144 V		90		
		f_{CM} = 60Hz, DR = 8 SPS		105		
		f_{CM} = 50Hz, DR = 8 SPS		105		
Digital Inputs / Outputs						
V_{OL}	Low-level output voltage	I_{OL} = 3 mA	GND	0.15	0.4	V
V_{IL}	Low-level input voltage		GND		0.3 × DVDD	V
V_{IH}	High-level input voltage		0.7 × DVDD		5.5	V
	Input leakage		-10		10	µA
Power Supply						
I_{VDD}	Supply current	Power down		0.5	2	mA
		Operating-continuous		150	200	
PD	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

10.5. Timing Requirements: I²C

Over operating ambient temperature range and VDD = 2.0 V to 5.5 V (unless otherwise noted)

Parameter		Fast mode		High-speed mode		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0.01	0.4	0.01	3.4	MHz
t_{BUF}	Bus free time between START and STOP condition	600		160		ns
t_{HDSTA}	Hold time after repeated START condition. First clock is generated after this period	600		160		ns
t_{SUSTO}	Setup time for STOP condition	600		160		ns
t_{HDDAT}	Data hold time	0		0		ns
t_{SUDAT}	Data setup	100		10		ns
t_{LOW}	Low period of the SCL clock pin	1300		160		ns
t_{HIGH}	High period of the SCL clock pin	600		60		ns
t_F	Rise time for both SDA and SCL signals		300		160	ns
t_R	Fall time for both SDA and SCL signals		300		160	ns



I²C Interface Timing

10.6. Characteristics for LTD2118

Minimum and maximum specifications are measured from T_A = −40°C to +125°C; typical specifications are measured at T_A = 25°C; all specifications are measured at VDD = 3.3 V, AVSS = 0 V, data rate = 8 SPS, FSR = 2.048 V (unless otherwise noted).

Parameter		Conditions	Min	Typ	Max	Unit
Analog Inputs						
	Common-mode input impedance	FSR = ±6.144 V		8		MΩ
		FSR = ±4.096 V, FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V		22		MΩ
		FSR = ±4.096 V		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, FSR = ±0.256 V		0.71		
Performance						
	Resolution	No missing code	16			Bits
DR	Data rate		8, 16, 32, 64, 128, 256, 512, 1024			SPS
	Data rate variation		-10%		+10%	
INL	Integral non-linearity	DR = 8 SPS, FSR = ±2.048 V			1	LSB
	Offset error	FSR = ±2.048 V, differential inputs		±0.1	2	LSB
		FSR = ±2.048 V, single-ended inputs		±0.25		
	Offset drift	FSR = ±2.048 V, T_A = -40 to 125 ℃		0.002		LSB/℃
	Offset long-term drift	FSR = ±2.048 V, T_A = 125 ℃, 1000 hrs		±1		LSB
	Offset power supply rejection	FSR = ±2.048 V, DC supply variation		0.2		LSB/V
	Offset channel match	Match between any two inputs		0.6		LSB
	Gain effor	FSR = ±2.048 V, T_A = 25 ℃		0.01%	0.15%	
	Gain drift	FSR = ±0.256 V		7		ppm/℃
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V		5		
	Gain power supply rejection			10		ppm/V
	Gain match	Match between any two gains		0.01%	0.1%	
	Gain channel match	Match between any two inputs		0.01%	0.1%	
CMRR	Common-mode rejection ratio	DC, FSR = ±0.256 V		105		dB
		DC, FSR = ±2.048 V		100		
		DC, FSR = ±6.144 V		90		
		f_{CM} = 60Hz, DR = 8 SPS		105		
		f_{CM} = 50Hz, DR = 8 SPS		105		
Digital Inputs / Outputs						

V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2 × VDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × VDD			V
V_{IL}	Low-level input voltage		GND		0.2 × VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	-10		10	µA
I_L	Input leakage, low	V_{IL} = GND	-10		10	µA
Temperature Sensor						
	Operating range		-40		125	℃
	Temperature resolution			0.03125		℃/LSB
	Accuracy			0.4	±1	℃
Power Supply						
I_{VDD}	Supply current	Power down		0.5	2	mA
		Operating-continuous		150	200	
PD	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

10.7. Timing Requirements: Serial Interface

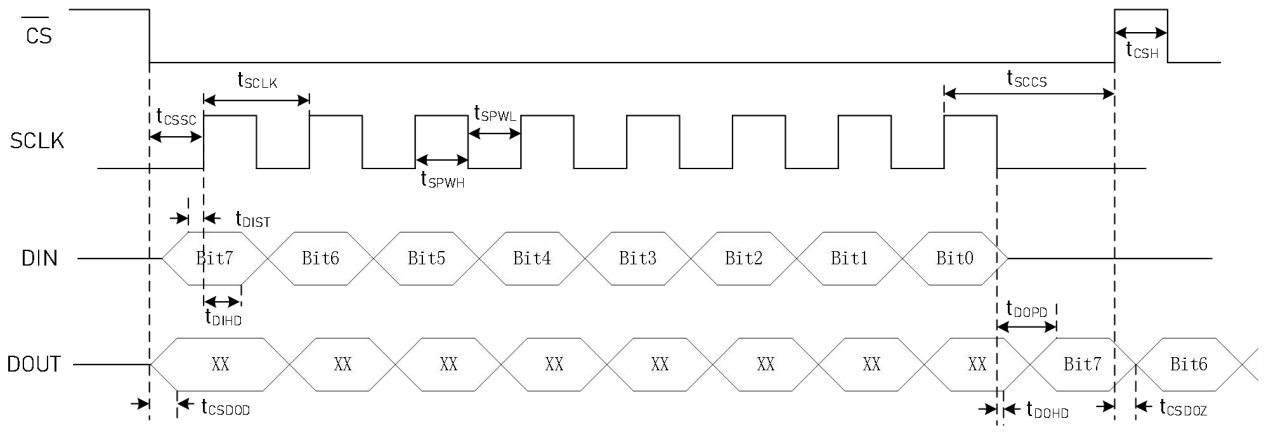
Over operating ambient temperature range and VDD = 2.0 V to 5.5 V (unless otherwise noted)

Parameter		MIN	MAX	UNIT
t_{CSSC}	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	100		ns
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWL}, t_{SPWH}	Pulse duration, SCLK high or low	100		ns
t_{SCCS}	Delay time, last SCLK falling edge before $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

10.8. Switching Characteristics: Serial Interface

Over operating ambient temperature range, load: 20 pF || 100 kΩ to GND.

Parameter		MIN	TYP	MAX	UNIT
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	0		50	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid DOUT			40	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance			50	ns



Serial Interface Timing