1. General Description

The LTD2284 is a 32-bit resolution, high-performance, analog-to-digital converter (ADC). It provides high resolution and low power operation modes to offer a trade-off between power consumption and SNR performance. It consists of a two-channel multiplexer, a low-noise programmable gain amplifier (PGA), a 4th-order delta-sigma (Δ-Σ) modulator and a programmable digital filter combination. It is SPI-compatible.

The two-channel differential-input multiplexer allows multiple configurations including two differential inputs and internal self-test modes.

The PGA has high input impedance and low noise, capable of small-signal applications. Chopper stabilization is incorporated to minimize the offset, offset drifts, and 1/f noise.

The fourth-order, inherently stable modulator provides outstanding noise and linearity performance. The modulator output is filtered and decimated by the on-chip digital filter to yield the ADC conversion result.

The digital filter provides data rates from 250 to 4000 SPS. Combinations of on-chip sinc filter, finite-impulse response (FIR) filter and high-pass filter (HPF) provides options for higher resolution or higher data rate. Gain and offset scale registers support system calibration.

The synchronization function allows external event triggering for ADC conversion as well as multiple LTD2284 together when applied synchronized pulses. The power-down input puts the ADC into power-down mode to minimize power and resets the register settings. SPI compatibility allows parallel ADCs sharing a common serial bus.

The LTD2284 is available in a compact 24-lead, 5 mm × 4 mm QFN package, and is fully specified from -40℃ to +85℃, with a maximum operating temperature range of -50℃ to +125℃.

2. Features and Benefits

- Selectable Operating Modes
- Low-Power Mode:
  - 12 mW (PGA = 1, 2, 4 and 8)
  - 128 dB SNR (250 SPS, PGA = 1)
- High-Resolution Mode:
  - 18 mW (PGA = 1, 2, 4 and 8)
  - 130 dB SNR (250 SPS, PGA = 1)
- THD: －120 dB
- CMRR: 110 dB
- Two-Channel Differential Multiplexer
- Low Noise Programmable Gain Amplifier
- Inherently-Stable 4th-order Δ-Σ Modulator
- Fast Responding Overrange Detector
- Flexible Digital Filter:

- Sinc + FIR + IIR (Selectable)
- Linear or Minimum Phase Option
- Programmable High-Pass Filter

- Offset and Gain Calibration
- Synchronization function
- SPI compatibility
- Analog Supply: 5 V
- Digital Supply: 1.8 V to 3.3 V

3. Applications

- Energy Exploration
- Seismic Monitoring
- High-Accuracy Instrumentation

4. Pin Configuration (Top View)

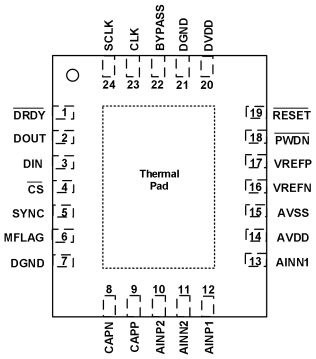

Fig. 1 Pin Configuration

5. Revision History

Version 0

Initial version.

Table of Contents

List of Figures

List of Tables

6. Pin Description

Symbol	Pin No.	I/O	Description
AINN1	13	Analog input	Negative analog input 1
AINN2	11	Analog input	Negative analog input 2
AINP1	12	Analog input	Positive analog input 1
AINP2	10	Analog input	Positive analog input 2
AVDD	14	Analog supply	Positive analog power supply
AVSS	15	Analog supply	Negative analog power supply
BYPAS	22	Analog	1.8 V sub-regulator output: connect 1 µF capacitor to DGND
CAPN	8	Analog	PGA output: connect 10 nF capacitor from CAPP to CAPN
CAPP	9	Analog	PGA output: connect 10 nF capacitor from CAPP to CAPN
CLK	23	Digital input	Master clock input (4.096 MHz)
$\overline{CS}$	4	Digital input	Serial interface chip select, active low
DGND	7	Ground	Digital ground (tie to digital ground plane)
DGND	21	Ground	Digital ground (tie to digital ground plane)
DIN	3	Digital input	Serial interface data input
DOUT	2	Digital output	Serial Interface data output
$\overline{DRDY}$	1	Digital output	Data ready output: active low
DVDD	20	Digital supply	Digital power supply. If DVDD < 2.25 V, connect DVDD and BYPAS pins together.
MFLAG	6	Digital output	Modulator overrange flag: 0 = normal, 1 = modulator overrange
$\overline{PWDN}$	18	Digital input	Power-down input, active low
$\overline{RESET}$	19	Digital input	Reset input, active low
SCLK	24	Digital input	Serial interface shift clock input
SYNC	5	Digital input	Synchronize input, rising edge active
VREFN	16	Analog input	Negative reference input
VREFP	17	Analog input	Positive reference input
Thermal pad			Do not electrically connect the thermal pad. The thermal pad must be soldered to PCB. Thermal pad vias are optional and can be removed.

7. Functional Block Diagram

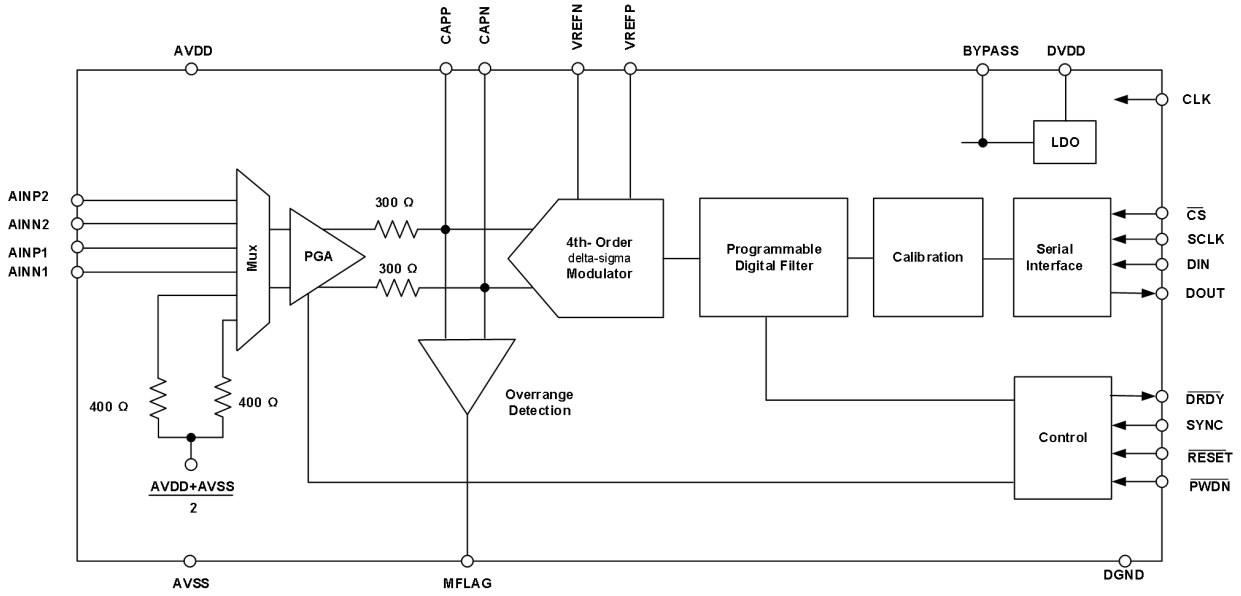

Fig. 2 Functional Block Diagram

8. Ordering Information

Part Number	Package Type	Quantity	Mark Code
LTD2284XF24/R10	QFN4×5-24L	Tape and Reel, 5000	D2284

9. Limiting Value

Parameter	MIN	MAX	UNIT
AVDD to AVSS	-0.3	5.5	V
AVSS to DGND	-2.8	0.3	V
DVDD to DGND	-0.3	3.9	V
Analog input voltage	AVSS-0.3	AVDD+0.3	V
Digital input voltage to DGND	-0.3	DVDD+0.3	V
Input current, continuous	-10	10	mA
Operating temperature	-50	125	°C
Junction temperature		150	°C
Storage temperature, Tstg	-60	150	°C

10. ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	

11. Recommended Operation Conditions

Parameter		Min	Typ	Max	Unit
Power Supply					
AVSS	Negative analog supply (relative to DGND)	–2.6		0	V
AVDD	Positive analog supply (relative to AVSS)	AVSS + 4.75		AVSS + 5.25	V
DVDD	Digital supply (relative to DGND)	1.65		3.6	V
Analog Inputs					
FSR	Full-scale input voltage range (VIN=AINP – AINN)		$\pm V_{REF}/(2\times PGA)$		V
	Calibration margin			106	%FSR
AINX	Absolute input voltage range	AVSS + 0.7		AVDD – 1.25	V
Voltage Reference Inputs					
V_{REF}	Reference input voltage (VREF = VREFP – VREFN)	1	5	AVDD – AVSS + 0.2	V
VREFN	Negative reference input	AVSS – 0.1		VREFP – 1	V
VREFP	Positive reference input	VREFN + 1		AVDD + 0.1	V
Digital Inputs					
V_{IH}	High-level input voltage	0.8 × DVDD		DVDD	V
V_{IL}	Low-level input voltage	DGND		0.2 × DVDD	V
f_{CLK}	Clock input	1		4.096	MHz
f_{SCLK}	Serial clock rate			f_{CLK} / 2	MHz

12. Electrical Characteristics

Maximum and minimum specifications over –40°C to +85°C; typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, High-Resolution and Low-Power modes, Offset enabled (75 mV), Chop enabled, and f_{DATA} = 1000 SPS (unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Unit
Analog Inputs						
	PGA input voltage noise density	Low-power mode		7.5		nV/ √Hz
		High-resolution mode		5		
	Differential input impedance	CHOP enabled		1		GΩ
		CHOP disabled		100		
	Common-mode input impedance			1		GΩ
I_{IB}	Input bias current			1		nA
	Crosstalk	f = 31.25 Hz		-135		dB
	Mux switch on-resistance	Each switch		30		Ω
PGA Output (CAPP, CAPN)						
	Absolute output range		AVSS + 0.4		AVDD – 0.4	V
	PGA output impedance	Differential		600		Ω
	Output impedance tolerance			±10%		
	External bypass capacitance			10	100	nF
	Modulator input impedance	Low-power mode		110		kΩ
		High-resolution mode		55		
AC Performance						
SNR	Signal-to-noise ratio	Low-power mode	117	122		dB
		High-resolution mode	120	124		
THD	Total harmonic distortion	Low-power mode				dB
		PGA = 1, 2, 4, 8, 16		-122	-108	
		PGA = 32		-117	-108	
		PGA = 64		-114		
		High-resolution mode				

		PGA = 1, 2, 4, 8, 16		-122	-107	dB
		PGA = 32		-117	-110	
		PGA = 64		-114		
SFDR	Spurious-free dynamic range			123		dB
DC Performance						
	Resolution		31			Bits
f_{DATA}	Data rate	FIR filter mode	250		4000	SPS
		Sinc filter mode	8000		128000	
	Offset	Offset disabled		±50	±200	µV
		Offset and Chop disabled		300		
		75 mV offset	70 / PGA	75 / PGA	80 / PGA	mV
		100 mV offset	95 / PGA	100 / PGA	105 / PGA	
	Offset after calibration			1		µV
	Offset drift			0.03		µV/°C
		CHOP disabled		0.5		
	Gain error	Low-power mode	-2%	-1.0%	0%	
		High-resolution mode	–2.5%	–1.5%	–0.5%	
	Gain error after calibration			0.0002%		
	Gain drift	PGA = 1		2		ppm/°C
		PGA = 16		9		
	Gain matching			0.3%	0.8%	
CMR	Common-mode rejection	f_{CM} = 60Hz, 1.25V_{PP}		114		dB
PSR	Power-supply rejection	f_{PS} = 60Hz, 100 mV_{pp}, AVDD, AVSS	80	90		dB
		f_{PS} = 60Hz, 100 mV_{pp}, DVDD	90	115		
Voltage Reference Inputs						
	Reference input impedance	Low-power mode		170		kΩ
		High–resolution mode		85		
Digital Filter Response						
	Pass-band ripple				±0.003	dB
	Pass band (–0.01 dB)			0.375×f_{DATA}		Hz
	Bandwidth (–3 dB)			0.413×f_{DATA}		Hz
	High-pass filter corner		0.1		10	Hz
Digital Filter Response						
	Pass-band ripple				±0.003	dB
	Pass band (–0.01 dB)			0.375×f_{DATA}		Hz
	Bandwidth (–3 dB)			0.413×f_{DATA}		Hz
	High-pass filter corner		0.1		10	Hz
	Stop band attenuation		135			dB
	Stop band			0.50×f_{DATA}		Hz
	Group delay	Minimum phase filter		5 / f_{DATA}		s
		Linear phase filter		31 / f_{DATA}		
	Settling Linear phase filter	Minimum phase filter		64/ f_{DATA}		s
		Linear phase filter		64/ f_{DATA}		
Digital Inputs / Outputs						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8×DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.2×DVDD	V
I_{lkg}	Input leakage	0<$V_{DIGITAL\ IN}$ < DVDD			±10	µA
Power Supply						
I_{AVDD} I_{AVSS}	Analog supply current	Low-power mode				
		PGA = 1, 2, 4, 8		2.5	3.4	mA
		PGA = 16, 32, 64		3	3.8	
		High-resolution mode				
		PGA = 1, 2, 4, 8		3.2	5.5	mA

		PGA = 16, 32, 64		4	6	
I_{DVDD}	Digital supply current	Low-power mode		0.4	0.7	mA
		High-resolution mode		0.6	0.8	
PD	Power dissipation	**Low-power mode**				
		PGA = 1, 2, 4, 8		12	20	mW
		PGA = 16, 32, 64		16	22	
		High-resolution mode				
		PGA = 1, 2, 4, 8		18	30	mW
		PGA = 16, 32, 64		22	33	
Timing						
t_{CSSC}	CS low to SCLK high: setup time		40			ns
t_{SCLK}	SCLK period		2		16	$1 / f_{CLK}$
$t_{SPWH, L}$	SCLK pulse duration, high and low		0.8		10	$1 / f_{CLK}$
t_{DIST}	DIN valid to SCLK high: setup time		50			ns
t_{DIHD}	Valid DIN to SCLK high: hold time		50			ns
t_{CSH}	CS high pulse		100			ns
t_{sccs}	SCLK high to CS high		24			$1 / f_{CLK}$
t_{CSDOD}	CS low to DOUT driven: propagation delay				60	ns
t_{DOPD}	SCLK low to valid new DOUT: propagation delay	Load on DOUT = 20 pF || 100 kΩ			100	ns
t_{DOHD}	SCLK low to DOUT invalid: hold time		0			ns
t_{CSDOZ}	CS high to DOUT tristate				40	ns

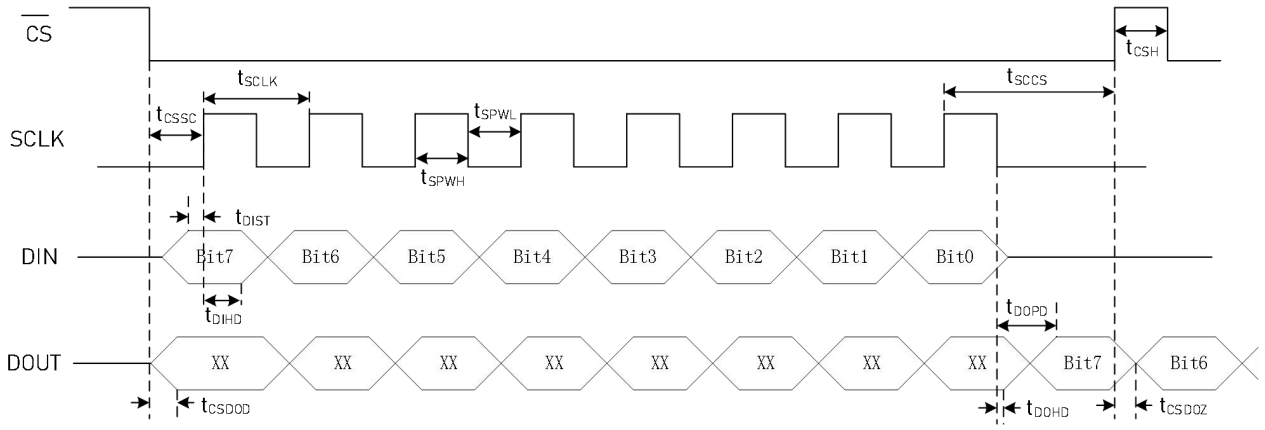

Fig. 3 Serial Interface Timing Diagram

13. Typical Characteristics

At +25 ℃, AVDD = 5 V, AVSS = 0 V,f_{CLK} = 4.096 MHz, VREFP = 5 V, VREFN = 0 V, DVDD = 3.3 V,PGA = 1, High-Resolution Mode, OFFSET enabled, CHOP enabled, and f_{DATA} = 1000 SPS (unless otherwise noted)

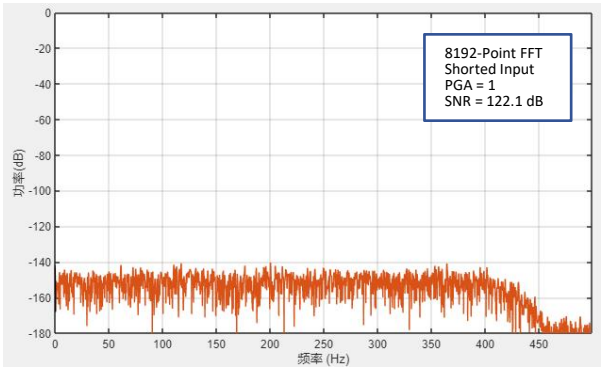

Fig. 4 Noise vs. Freq. @ PGA=1, CHOP Enabled

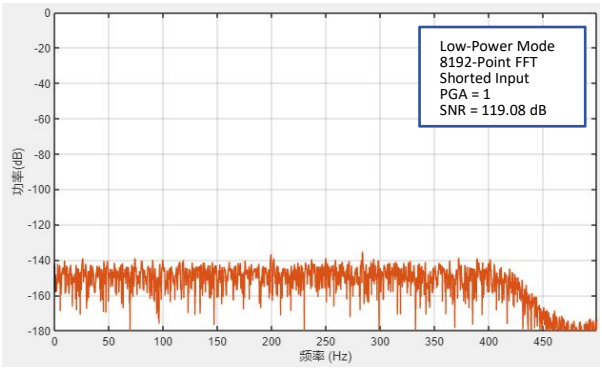

Fig. 5 Noise vs. Freq. @ PGA=1, CHOP Enabled (Low Power Mode)

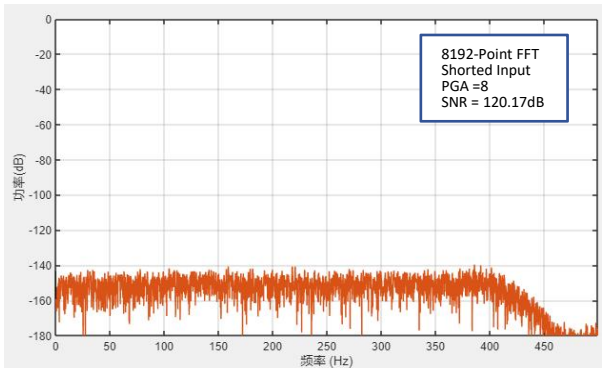

Fig. 6 Noise vs. Freq. @ PGA=8, CHOP Enabled

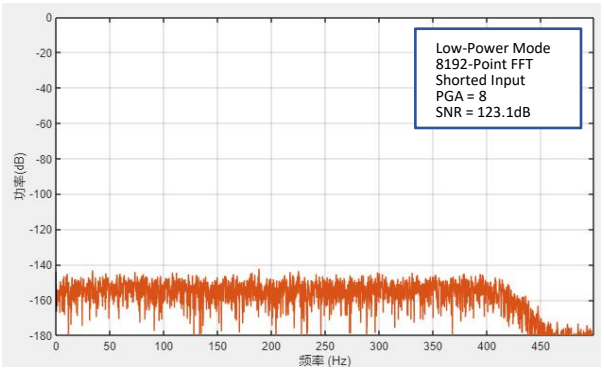

Fig. 7 Noise vs. Freq. @ PGA=8, CHOP Enabled (Low Power Mode)

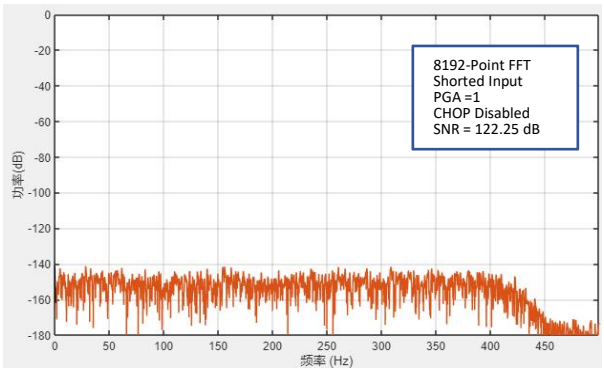

Fig. 8 Noise vs. Freq. @ PGA=1, CHOP Disabled

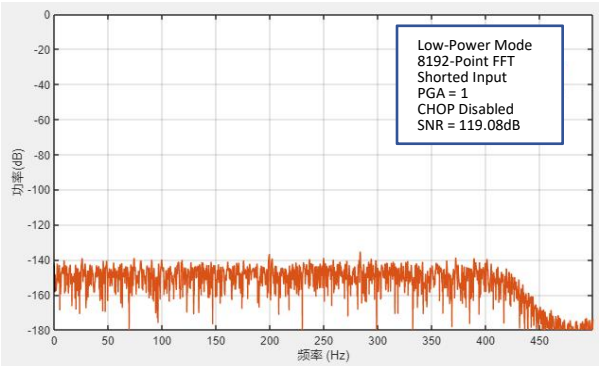

Fig. 9 Noise vs. Freq. @ PGA=1, CHOP Disabled (Low Power Mode)

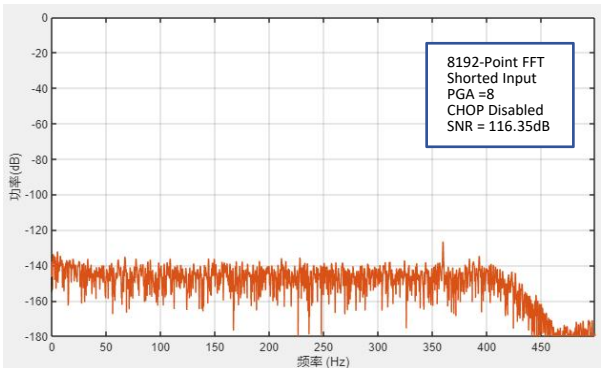

Fig. 10 Noise vs. Freq. @ PGA=8, CHOP Disabled

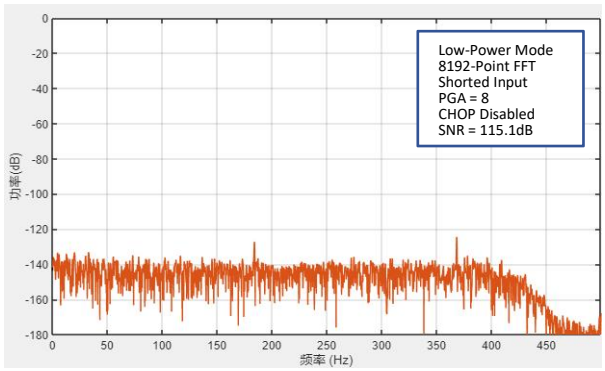

Fig. 11 Noise vs. Freq. @ PGA=8, CHOP Disabled (Low Power Mode)

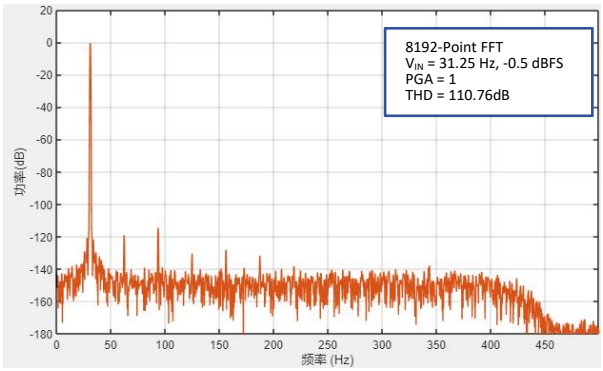

Fig. 12 Harmonics vs. Freq. @ PGA=1

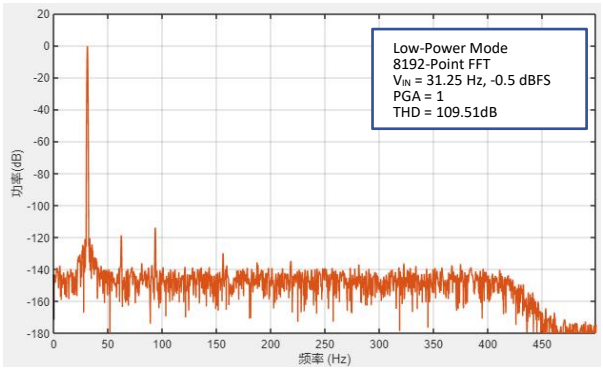

Fig. 13 Harmonics vs. Freq. @ PGA=1 (Low Power Mode)

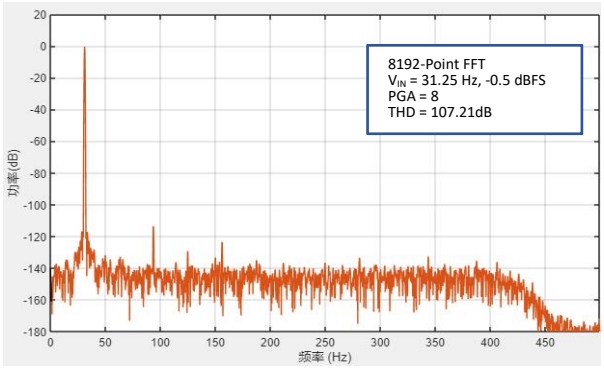

Fig. 14 Harmonics vs. Freq. @ PGA=8

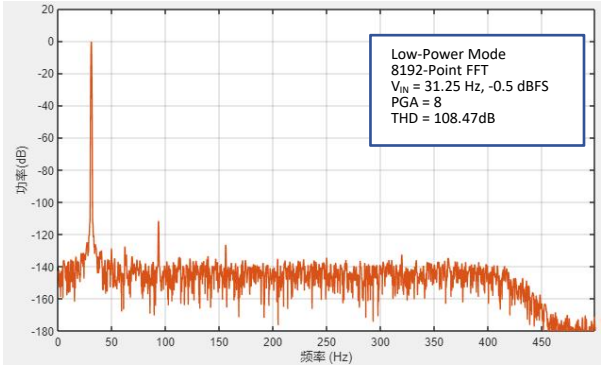

Fig. 15 Harmonics vs. Freq. @ PGA=8 (Low Power Mode)

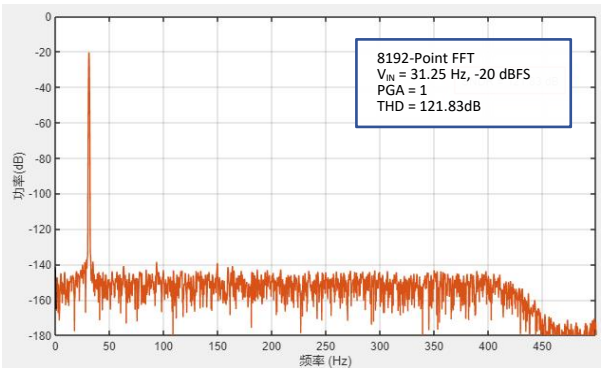

Fig. 16 Harmonics vs. Freq. @ PGA=1, Smaller Input

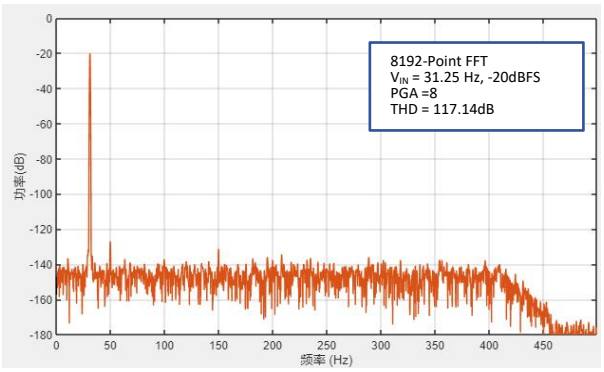

Fig. 17 Harmonics vs. Freq. @ PGA=8, Smaller Input

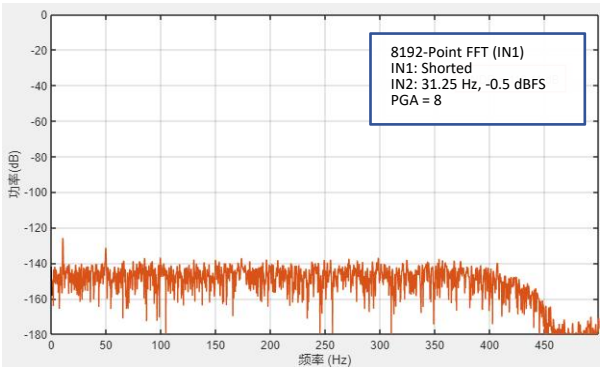

Fig. 18 Crosstalk Spectrum

14. Detailed Description

14.1. Analog Inputs and Multiplexer

Analog inputs are protected by ESD diodes. The input voltage is clamped between AVSS - 0.3 V and AVDD + 0.3 V, and once it overranged the protection diodes are on. External clamp diodes, series resistors, or combination of both could be used to limit the input current to its allowable values. Overdriving one unused input can affect the conversion of the other input. External Schottky diodes can be uesd to prevent the interaction between overdriven input and measured input by clamping the overdriven signal.

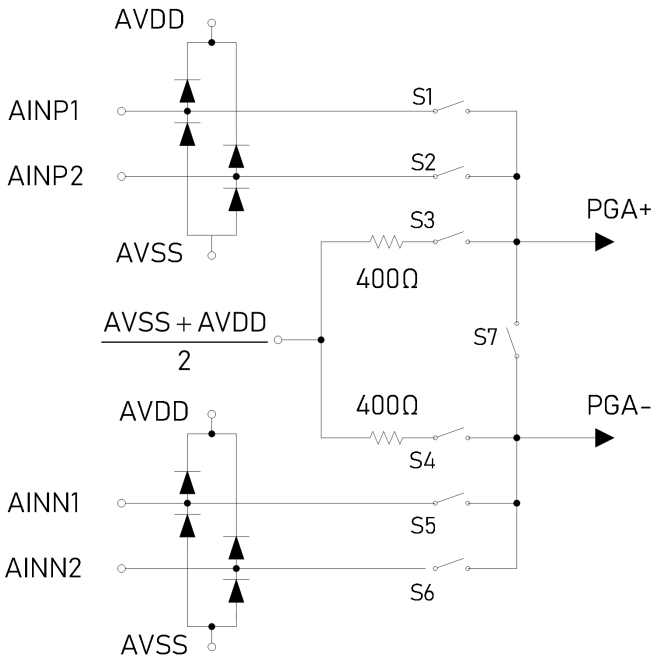

Fig. 19 Analog Input Multiplexer

The multiplexer provides different modes to connects one or two of the differential inputs to the preamplifier or self-test modes. Following table summarizes the configurations

Table 1 Mux. Configuration

MUX[2:0] @ CONFIG1 (address=02h)	Description
000	AINP1 and AINN1 (default)
001	AINP2 and AINN2
010	Internal short through 400-Ω resistor
011	AINP1 and AINN1 connected to AINP2 and AINN2
100	External short to AINN2

14.2. Programmable Gain Amplifier

LTD2284 integrated a low-noise, differential-in and -out programmable gain amplifier (PGA). The gain of PGA can be set by register bits PGA[2:0], adjustable from 1 to 64 times to meet different full-scale requirements. Following table shows the PGA settings with their corresponding gain and range.

Table 2 PGA Configuration		
PGA[2:0] @ CONFIG1 (address=02h)	Gain	Differential input range (V)
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.312
100	16	±0.156
101	32	±0.078
110	64	±0.039

The PGA drives the Δ-Σ modulator through 300 Ω internal resistors. The input impedance of the modulator varies with operation mode. The input impedance of high-resolution mode is about 55 kΩ while low-power mode doubles the value (by design). A 10 nF capacitor must be connected between CAPP and CAPN in order to filter sampling glitches meanwhile serves as antialias filter whose corner frequency can be expressed as following equation:

$$f_P = \frac{1}{3780 \times C}$$

Chopping structure is incorporated for stabilization where the offset, offset drift and 1/f noise are removed from pass-band frequency range as shown in . Chopping function can be disabled by setting CHOP bit to 0 at the CONFIG1 (address = 02h) and PGA input impedance increases accordingly. The input impedance of PGA decreases as the gain increases. Following table gives the relations between PGA and differential input impedance.

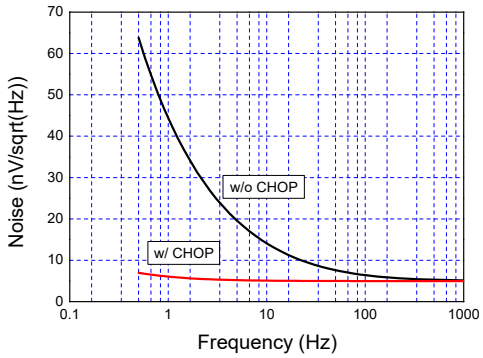

Fig. 20 PGA Noise w/ and w/o Chopping

Table 3 Differential Input Impedance of Gains	
PGA	Differential input impedance (GΩ)
1	7
2	7
4	4
8	3
16	2
32	1
64	0.5

Considering the charges stored on stray capacitance of the input chopping switches, low-level transient currents can flow through inputs when chopping is enabled. Such currents may may have influence on the conversion when used high-impedance sensors or termination resistors which is comparable to the input impedance of the PGA. In such cases, ADC performances may be improved by disabling chopping.

14.3. Analog-to-digital Converter

The analog-to-digital converter (ADC) consists of a 4th-order, low-noise modulator and a programmable digital fiter.

14.3.1. The 4th-order, Low-noise Modulator

The 4th-order, low-noise modulator shifts the quantization noise to a higher frequency, out of passband, that can be removed by the digital filter. Flexible options either to be completely filtered by integrated on-chip digital filters or partially filtered by sinc filter only. External FIR filter can be used after internal sinc filter. The chopping frequency is set to be 4 kHz intended to optimize the modulator performance in the range from DC to 2 kHz, resulting in spectral artifact at 4 kHz and its harmonics. When considering using external FIR filter, design should be done to suppress the chopping artifacts.

14.3.1.1. Modulator Over-range

Modulator over-range is predictable due to the unique design of the modulator, that makes it inherently stable. Instead of having self-reset cycle during which it will output unstable data stream. LTD2284 is designed to output a data stream with 90% duty cycle of ones-to-zeroes density with the positive full scale input and 10% with the nagative full scale. When input is overdriven while not saturated, the modulator continues to output stable data stream. The output codes may not clip to positive or negative full scale depending on the overdriven duration. After the input signals go back within the normal range, the modulator returns to normal range immediately. However the group delay of the digital filter postpones the conversion data to be within the linear range about 31 readings for linear phase FIR. 62 readings are needed for completely settled data.

14.3.1.2. Modulator Input Impedance

The input impedance is about 55 kΩ in high-performance mode and about 110 kΩ in low-power mode. It samples the buffered input voltage through an internal capacitor. This input impedance and PGA output resistors result in systematic gain errors. The capacitor and PGA output resistors can vary up to ±20% due to production deviation.

14.3.1.3. Modulator Over-range detection (MFLAG)

There is a fast-responding detection circuitry triggered when differential input exceeds positive or negative full scale, and outputs high voltage.The threshold tolerance is set to ±2.5%. The MFLAG output is sampled at the rate of $f_{MOD}/2$, as a result, the minimum MFLAG pulse duration is $2/f_{MOD}$.

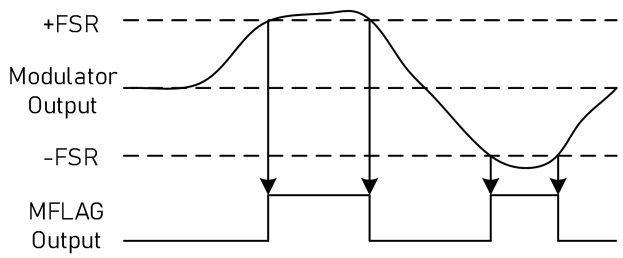

Fig. 21 Modulator Over-range Flag Operation

14.3.1.4. Offset

An offset voltage can be manually added in order to shift the idle tones to the stop band of the digital filter response when there is no input signals or very low-level signal. This offset is applied at the modulator input, therefore the PGA gain has no effect on it. Two options, 75 mV and 100 mV, are provided. 75 mV offset is more effective to reduce idle tones under various gain, data rate and chop mode settings. This function is enabled by OFFSET1 and OFFSET0 bits at ID_CFG register. This function will reduce the available full scale, but it can be restored by digital offset calibration.

14.3.1.5. Voltage Reference (VREFP, VREFN)

Voltage reference is applied by external source through VREFP and VREFN differentially. The reference inputs are protected by ESD diodes. The minimum operational input voltage is AVSS-0.3 V, and the maximum operational input voltage is AVDD+0.3 V. If the input reference voltage goes beyond the range, the protection ESD diodes may turn on and clip the input. The effective differential impedance of the reference input can be estimated by: $R_{EFF} = 1/f_{MOD} \times C_{IN}$

Following figure shows the simplified reference input circuit.

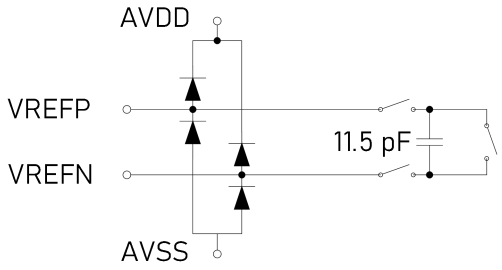

Fig. 22 Reference Input Circuit

Use a low-noise 5-V voltage reference helps LTD2284 achieve its best performance. Lower voltage reference can be used, however reduce the analog input range and degrade overall system performance. The circuitry provide reference voltage including noise filtering is critical to achieve better performance.

14.3.2. Digital Filter

Digital filter receives, decimates and filters the modulator output data stream. Tradeoffs can be made between resolution and data rate. The digital filter consists of a variable-decimation sinc filter, a fixed decimation FIR, a low-pass fiter with selectable phase option and a programmable high-pass filter.

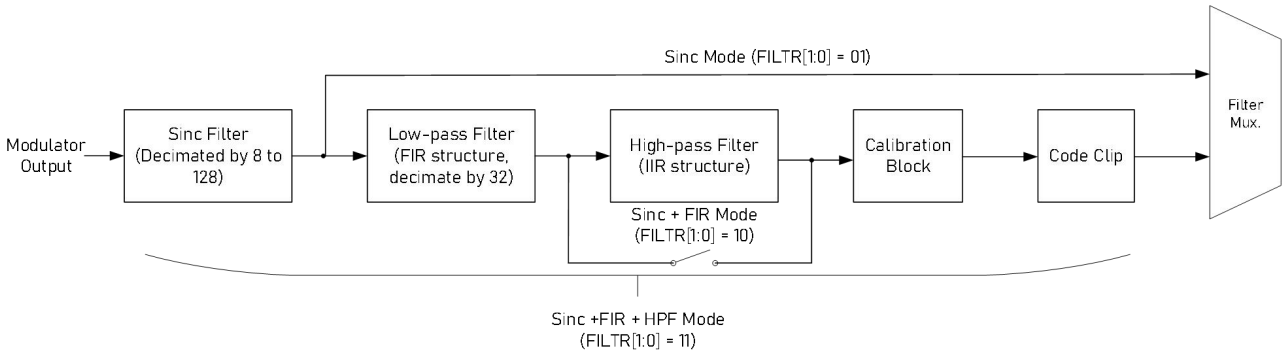

Fig. 23 Digital Filter Configuration

The digital filter can switch from partially filtering or complete filtering. Sinc filtering mode is designed to be used with external FIR filter. Sinc and FIR filtering mode is designed for complete on-chip filtering, and the HPF can be included to remove dc and low frequencies. Following table shows the digital filter configuration.

Table 4 Digital Filter Selection

FILTR[1:0] @CONFIG0 (address=01h)	Digital filter mode
00	Reserved (not used)
01	Sinc
10	Sinc+FIR
11	Sinc+FIR+HPF

14.3.2.1. Sinc Filter Section (sinx/x)

Sinc filter section (sinx/x) is a variable decimation rate, fifth-order, low-pass filter. Data stream comes into the filter at the rate of $f_{mod}=f_{clk}/4$ in high-resolution mode or $f_{clk}/8$ in low-power mode. The sinc filter suppresses the high-frequency noise produced by the modulator and meanwhile reduces the data rate by decimation. The decimation ratio is programmable through DR[2:0] bits shown as below

Table 5 Sinc Filter Mode Data Rates

FILTR[1:0] @CONFIG0 (address=01h)	Decimation ratio (Sinc filter mode)		Data rate
	High-resolution mode	Low-power mode	
000	128	64	8000
001	64	32	16000
010	32	16	32000
011	16	8	64000
100	8	4	128000

The sinc filter is designed to have notches that occur at the output data rate and multiples. Frequency response of the sinc filter and the roll-off is shown as below

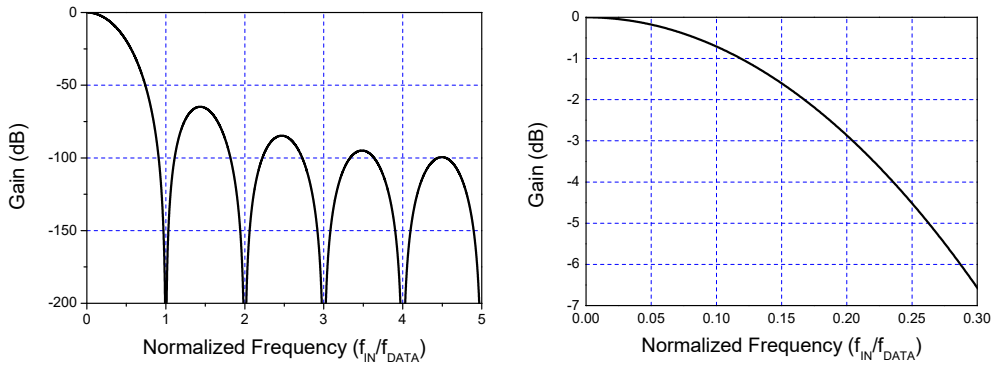

Fig. 24 a) Sinc Filter Frequency Response. b) Sinc Filter Roll-off.

14.3.2.2. FIR Low-pass Filter

FIR is the second section of the digital filter. Selection of linear phase mode and minimum phase mode is integrated and the total decimation ratio of this section is 32. The resulting overall decimation ratio and data rate is shown as below

Table 6 FIR Filter Data Rates

FILTR[1:0] @CONFIG0 (address=01h)	Overall decimation ratio (Sinc+FIR mode)		Data rate
	High-resolution mode	Low-power mode	
000	4096	2048	250
001	2048	1024	500
010	1024	512	1000
011	512	256	2000
100	256	128	4000

The frequency response of the FIR filter is flat to 0.375*f_{data} (±0.003dB pass-band ripple until 0.375*f_{data}) and is fully suppressed at the Nyquist frequency.

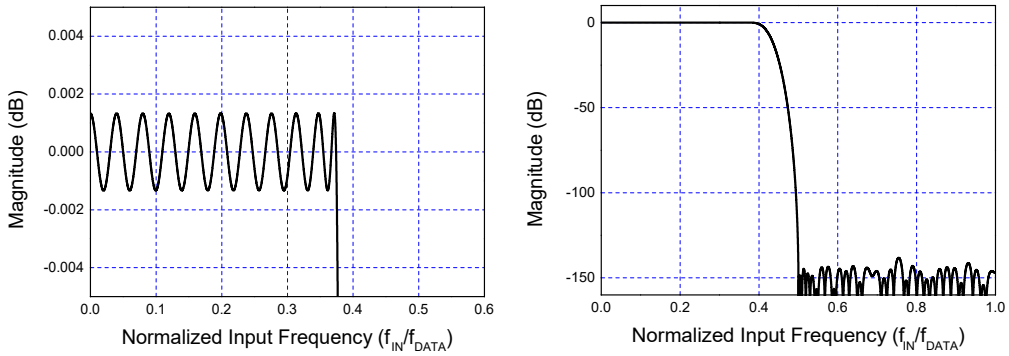

Fig. 25 a) FIR Pass-band Magnitude Response. b) FIR Transition Band Magnitude Response

14.3.2.3. Group Delay and Step Response

It is designed to be switchable between linear response and minimum phase response. The pass band, transition band and stop band responses of both filters are similar while differs in delay time. In linear phase mode, the delay is constant for any input signals to respective output data. When analyzing multi-tone signals, such configuration is necessary to have no phase error. On the other hand, minimum phase mode can help achieve shortest delay, however the phase relationship against frequency is not constant. This function is selected by PHASE bit as shown below:

Table 7 Phase Selection	
PHASE[1:0] @CONFIG0 (address=01h)	Step response
0	Linear
1	Minimum

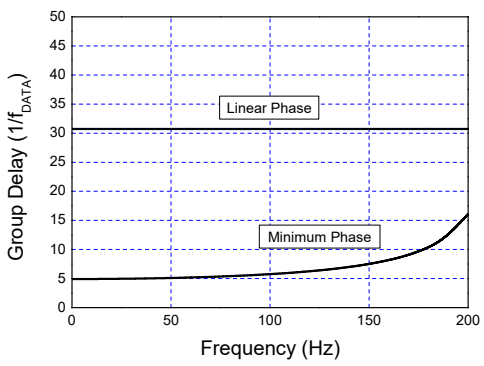

Fig. 26 FIR Group Delay (f_{DATA} = 500Hz)

14.3.2.4. High-pass Filter

The high-pass filter session is the last section of the digital filter as an IIR structure. Its corner frequency is programmable by HPF0 and HPF1 registers. The corner frequency can be tuned according to following function:

$$\mathrm{HPF}[1:0] = 65536 \times [1 - \sqrt{1 - 2 \times (\cos\omega_N + \sin\omega_N - 1)/\cos\omega_N}$$

Where: ω_N = $2\pi f_{HP} / f_{DATA}$, f_{HP} = High-pass filter corner frequency, f_{DATA} = Data rate.

Table 8 HPF[1:0] Value Examples

f_{HP} (Hz)	Data Rate (SPS)	HPF[1:0] Value
0.5	250	0337h
1	1000	019Ah

14.4. Functional Modes

14.4.1. Low Power Mode

LTD2284 supports high-resolution operation mode for best performance and low-power mode for power-sensitive application, such as battery charged devices and hand-held equipment. In low-power mode, the consumed current in different blocks through the conversion path can be modified and suppressed by the user. As a result, performance in SNR and THD sacrifices a little. The current consumed in low power mode scales down 30% comparing to high-resolution mode.

14.4.2. Synchronization

Either through SYNC pin or SYNC command, synchronization can be triggered by an external event, therefore synchronizing multiple LTD2284 devices is possible when applying trigger signal simultaneously. There are two synchronization modes: pulse-sync and continuous-sync. In pulse-sync mode, the device synchronizes whenever the synchronization event comes. In continuous-sync mode, the first synchronization is unconditional, thereafter the ADC re-synchronizes only when the next SYNC pin edge does not occur at an integer multiple of the data rate. When the periods of SYNC input and DRDY output do not match, the device re-synchronized.

14.4.2.1. Pulse-Sync Mode

This mode forces the device to stop the conversion and restart the process. Synchronization occurs on the next rising CLK edge after the rising SYNC edge, or after the eighth rising SCLK edge when by SYNC command.

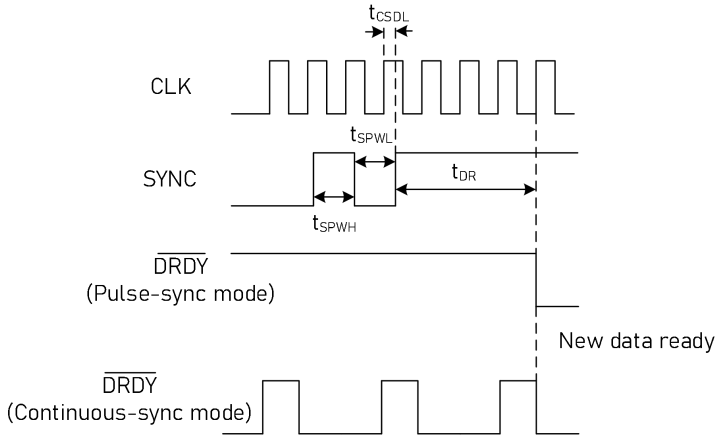

Fig. 27 Synchronization Timing with Single Pulse

Table 9 Synchronization Timing				
Parameter		Min	Max	Unit
t_{CSDL}	CLK rising edge to SYNC rising edge	30	-30	ns
t_{SYNC}	SYNC clock period	1	infinite	n/f_{DATA}
$t_{SPWH, L}$	SYNC pulse width, high or low	2		$1/f_{CLK}$
t_{DR}	Time for data ready (Sinc filter)	See next table		
	Time for data ready (FIR filter)	$64/f_{Data}$		

Table 10 t_{DR} for Data Ready (Sinc Filter)	
f_{Data} (kSPS)	t_{DR} (f_{CLK} cycles)
128	440
64	616
32	968
16	1672
8	2824

14.4.2.2. Continuous-Sync Mode

In continuous mode, either single pulse or continuous clock can be used to trigger synchronization by using SYNC pin. When the rising edge of single pulse comes in, it has the same behavior as the Pulse-Sync mode. The ADC only re-synchronizes when the time between adjacent rising edges is not a integer multiple of conversion period. Please note that there is phase difference between DRDY and applied clock due to internal delay. During re-synchronization, the DRDY pin keeps toggle, and the DOUT pin is held low until data are ready.

When enters continuous-sync mode, the first rising edge of SYCN triggers synchronization unconditionally. Any writes to the registers will result in re-synchronization. Re-synchronization will cause the loss of previous synchronization. By sending command STANDBY followed by WAKEUP, previous synchronization can be restored. Similarly, the time between the two commands should not be a multiple integer of the conversion period by at least one clock cycle.

14.4.3. Reset

Reset can be realized by on/off power supplies, pull down the $\overline{\text{RESET}}$ pin voltage or send RESET command. To force reset, $\overline{\text{RESET}}$ pin voltage should be kept low for at least $2/f_{clk}$ and released to start reset. By sending RESET command, reset starts when the next rising edge of SCLK comes after the eighth rising edge of SCLK. Registers will be set to their default value and the device starts synchronization at the next rising edge of CLK.

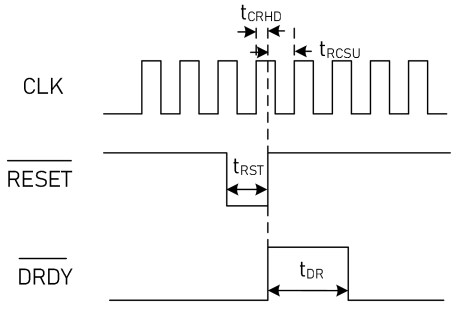

Fig. 28 Reset Timing

Table 11 Reset Timing			
Parameter		Min	Unit
t_{CRHD}	CLK to RESET hold time	10	ns
t_{RCSU}	RESET to CLK setup time	10	ns
t_{RST}	RESET low	2	$1/f_{CLK}$
t_{DR}	Time for data ready	$64/f_{DATA}$	s

14.4.4. Master Clock Input (CLK)

A high-quality, low-jitter clock is essential for optimum performance. The specified clock frequency is 4.096 MHz. Data rate scales with frequency but lowering the clock frequency do no benefits for noise reduction; select a lower data rate reduces noise. Make sure not to excess frequency and keep the trace as clean as possible. Use a 50 Ω series resistor close to the source.

Lowering the CLK frequency can help acquire a decreased power consumption (sacrificing AC performances). Contact Linearin for detailed measurement data under lower CLK frequency if desired.

14.4.5. Power-down ($\overline{\text{PWDN}}$ pin and STANDBY Command)

The device can manually powered down by pulling $\overline{\text{PWDN}}$ pin low or sending STANDBY command. The internal circuitry is therefore disabled to minimize the power consumption. Registers are reset after power-down. After STANDBY command is sent, the SPI port and configuration stay active. The device will switch on when $\overline{\text{CS}}$ is taken high.

14.4.6. Power-on Sequence

Following figure the power-on sequence of the device. It has 3 power supplies: AVDD, AVSS and DVDD. When all the supplies pass the power-on reset threshold, a period of $2^{16}/f_{CLK}$ will be counted before issuing the internal reset. Please note there is no specified order of the supplies. Once the new conversion after releasing the internal reset is finished, $\overline{\text{DRDY}}$ pin is pulled low.

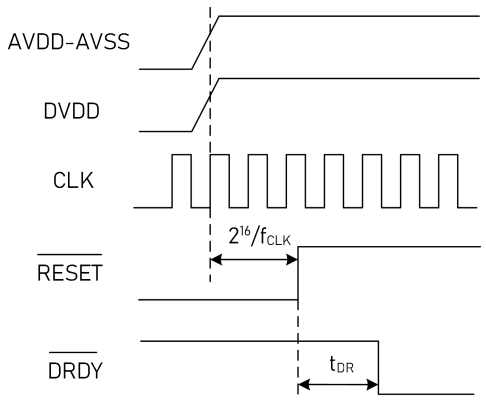

Fig. 29 Power-on Sequence

14.4.7. DVDD Power Supply

It operates from 1.65 V to 3.6V. In case that the device does not work properly under low supply voltage, connect

the DVDD input to BYPAS when supply voltage goes below 2.25 V, otherwise do not connect to this pin.

14.4.8. Serial Interface

Serial interface is used for reading converted data and to configure the related registers. It is SPI-compatible, and has four I/Os: SCLK, DIN, DOUT and $\overline{CS}$. By applying a 2.048 MHz clock to SCLK, 15 devices in total can work spontaneously sharing the common bus at data rate of 4k SPS.

14.4.8.1. Chip Select ($\overline{CS}$)

It disables the communication by pushing chip select pin high. When disabled, DOUT is high impedance. Also, any activities on SCLK pin will be ignored, data transfer and commands in progress be reset. $\overline{CS}$ should be kept low during data transfer, or tied low for permanently enabling. When it toggles high, the device quit the standby mode and continues data reading mode.

14.4.8.2. Serial Clock (SCLK)

Serial clock pin is to clock data in and data out through serial interface. It is designed as a Schmmitt-trigger input for noise immunity. Use a clean clock to prevent any accidentally introduced glitches that shift the data input or output. Data are shifted in at the rising edge and out at the falling edge.

14.4.8.3. Data Input (DIN) and Data Output (DOUT)

Data in and out pins are used for configuring registers, sending commands or reading data. Keep DIN pin low in read-data-continuous mode except sending SDATAC command.

14.4.8.4. Serial Port Auto Timeout

This feature is provided in order to automatically recover when data transmission is stopped or interrupt. This feature is useful when chip select is tied low. If manually recovering is required, pulled SCLK pin low for at least 64 $\overline{DRDY}$ cycles. Reset of the interface terminates the data transferring and command in progress. A new communication cycle starts at the rising edge of SCLK after reset occurs. As a result, to avoid force reset remotely, in every 64 $\overline{DRDY}$ cycles must have at least 1 pulse.

14.4.8.5. Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output pin to indicate the status of data retrieval. In continuous reading mode, read operation must be done in four CLK periods before the next falling edge, otherwise the data will be overwritten by the next conversion. In command mode, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. With data readback, $\overline{DRDY}$ resets on the first falling edge of SCLK. Without data readback, $\overline{DRDY}$ pulses high for four cycles during data updating. $\overline{DRDY}$ stays active when $\overline{CS}$ is high.

14.4.9. Data Format

The device outputs a 32-bit data in binary twos complement format. The LSB is a redundant bit to indicate the sign where 0 is for positive numbers and 1 for negative numbers. To be noted, if the output is clipped to +FS, LSB outputs 1, and when clipped to -FS, LSB outputs 0. If necessary, the data readback can be stopped at 24 bits.

Table 12 Ideal Output Code

VIN (VAINP - VAINN)	Output Code	
	FIR Filter	Sinc Filter
$> \frac{V_{REF}}{2PGA}$	7FFFFFFFh	Not defined
$= \frac{V_{REF}}{2PGA}$	7FFFFFFEh	3FFFFFFFh
$= \frac{V_{REF}}{2PGA \times (2^{30}-1)}$	00000002h	00000001h
0	00000000h	00000000h
$= \frac{-V_{REF}}{2PGA \times (2^{30}-1)}$	FFFFFFFFh	FFFFFFFFh
$= \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30}-1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30}-1}$	80000000h	Not defined

14.4.10. Reading Data

The device provides two modes to read conversion data: read-data-continuous mode and read-data-by-command mode.

14.4.10.1. Read-Data-Continuous Mode

In this mode, converted data can be read directly without receiving ready command. This mode is automatically entered after power-on or by sending RDATAC command. The data ready indicator $\overline{DRDY}$ is actively low. After $\overline{DRDY}$ is asserted, DOUT pin starts to output data serially. The data will be latched at the rising edge of SCLK. $\overline{DRDY}$ goes back to high at the first falling edge of SCLK. Till all the 32-bit data has been read, following SCLK signal will cause DOUT to stay logic low. The entire data shift operation must be completed within four CLK periods before $\overline{DRDY}$ is asserted once more, otherwise the data may corrupt.
When the stopping read-data-continuous SDATAC command is issued, the $\overline{DRDY}$ is tied high, however conversion continues internally. Data reading is done by command in this case.

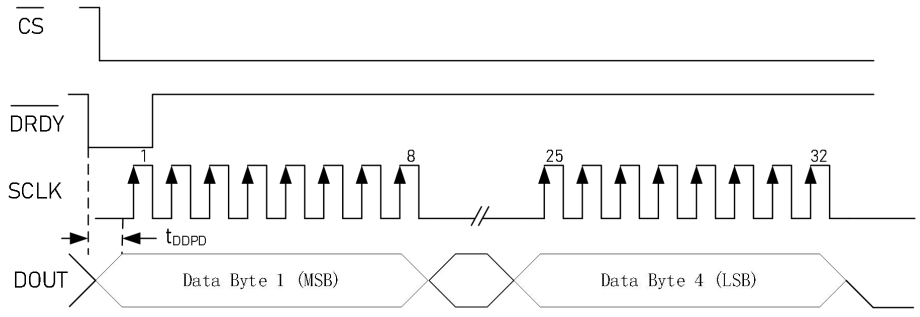

Fig. 30 Read-data-continuous Timing

Table 13 Reset Timing

Parameter		Min			Unit
t_{DDPD}	$\overline{DRDY}$ to valid MSB on DOUT propagation delay			100	ns

14.4.10.2. Read-Data-By-Command Mode

After receiving SDATAC command, the device enters read-data-by-command mode. In this mode, reading data is activated by RDATA command. When the last bit of RDATA command is received (on the eighth CLK rising edge), DOUT starts to output converted data once $\overline{DRDY}$ is asserted after a $\overline{DRDY}$ -to-MSB propagation delay. The data will be latched at the rising edge of SCLK.

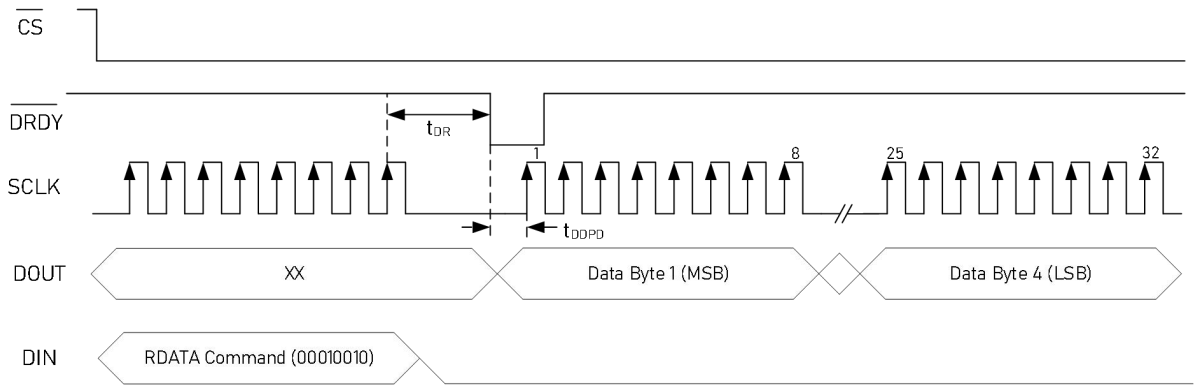

Fig. 31 Read Data by Command Timing

14.4.11. One-shot Conversion

The device can operate in one-shot conversion mode. By issuing STANDBY command, the device enters a power-saving standby mode. To start a one-shot conversion, send WAKEUP command. The converted data is ready to read once the $\overline{DRDY}$ is asserted. Then send a STANDBY command to go back to standby mode and wait for the next one-shot conversion by repeating the cycle.

14.4.12. Calibration Registers of Offset and Full-scale

Before final output stage, the converted data can be further modified through offset and gain calibration. The final output is first subtracted by the coefficient stored in the offset register (OFC) and then multiplied by the coefficient stored in full-scale register (FSC). Following equation shows the modification:

$$\text{Modified final output} = (\text{Modulator output} - \text{OFC}[2{:}0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}}$$

Both values stored in these two registers can be set by direct writing, or by calibration commands automatically. Changing PGA settings usually requires re-calibration. To be noted, calibration is bypassed in sinc filter mode.

14.4.12.1. OFC[2:0] Registers

The offset calibration coefficient is stored in three 8-bit registers, and is left-justified to align with the 32 bits of the conversion data. It is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. The default value is 000000h for no offset correction.

14.4.12.2. FSC[2:0] Registers

The full-scale coefficient is stored in three 8-bit registers, straight binary coded, normalized to unit gain at 400000h.

14.4.13. Calibration Commands

The calibration commands OFSCAL and GANCAL can be used to automatically obtain the coefficients to calibrate

the converted data before final output. It is recommended to input appropriate signals before sending the commands. If necessary, use a lower data rate to obtain a more accurate calibration coefficient by taking the advantage of less significant noise level under lower data rate. If calibration process is desired right after power-on, use should take note that the reference voltage is fully stabilized.

Following figure shows the calibration command sequence. After analog input and reference voltage are stabilized, send SDATAC, SYNC and RDATAC commands sequentially. $\overline{DRDY}$ will switch to logic low after 64 data periods, and afterwards send SDATAC, calibration command (either OFSCAL or GANCAL), and RDATAC sequentially. After 16 data periods, calibrations is finished, and conversion data can be read. SYNC input must be tied to logic high during calibration.

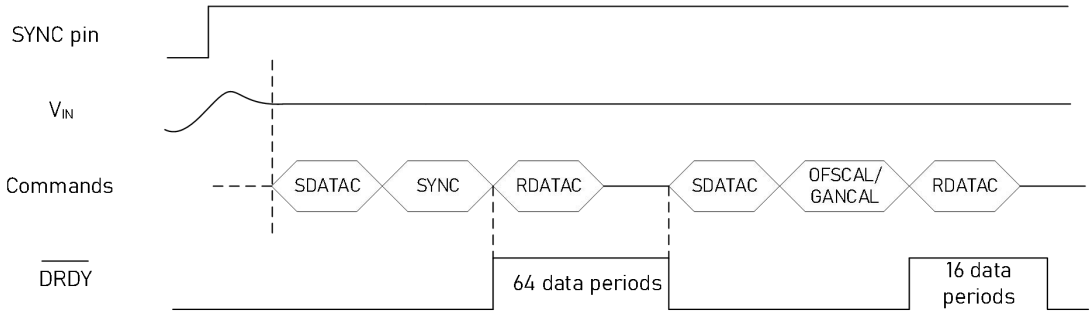

Fig. 32 Calibration Timing

Theoretically, every set of coefficients are corresponding to specific PGA settings, therefore, re-calibration is supposed to executed every time when PGA is changed.

14.4.13.1. OFSCAL Command

The user must provide a zero input signal to the input of the device before calibrating the offset. The device averages 16 readings, and write this value internally to the OFS register. If the optional 100-mV or 75-mV offset is applied, use this command to compensate.

14.4.13.2. GANCAL Command

The user must provide a stable full-scale DC signall to the input of the device before calibrating the offset. The device averages 16 readings, and calculate the coefficient to achieve full-scale, and then write internally to the OFS register.

14.4.14. Manual Calibration

Both OFSCAL and GANCAL registers can be read and written by the user to manually calibrate the converted data. Recommended steps are provided as following:

1) Set both registers to the default values, i.e. 0h and 400000h respectively.
2) Apply a zero differential signal to the input, and average the output readings and write this value to OFSCAL register.
3) Apply a differential DC signal or an AC signal, and average the output readings. Calculate the coefficient and write to GANCAL register. Equation is give below:

$$FSC[2:0] = 4000000h \times \frac{Expected\ Output\ Code}{Actual\ Output\ Code} \quad \text{for DC input.}$$

$$FSC[2:0] = 4000000h \times \frac{Expected\ Output\ RMS}{Actual\ Output\ RMS} \quad \text{for AC input.}$$

14.5. Programming

14.5.1. Commands List and Description

Following table lists the commands to control LTD2284. The device must be selected first ($\overline{CS}$ remains logic low) to receive the commands. A delay of 24 $1/f_{CLK}$-cycles is required between every byte within single command or between commands, counting from the last rising edge of the previous byte to the first rising edge of the following byte.

Table 14 Command List

Command	Type	Description	1st byte	2nd byte
WAKEUP	Control	Recover from standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter standby mode	0000 001X (02h or 03h)	
SYNC	Control	Synchronize the AD conversion	0000 010X (04h or 05h)	
RESET	Control	Reset registers to default value	0000 011X (06h or 07h)	
RDATAC	Control	Enter data-read-continuous mode	0001 0000 (10h)	
SDATAC	Control	Stop data-read-continuous mode	0001 0001 (11h)	
RDATA	Data	Read data by command	0001 0010 (12h)	
RREG	Register	Read *nnnnn* registers at address *yyyyy*	001*n nnnn* (20h+000*n nnnn*)	000*y yyyy* (00h+000*y yyyy*)
WREG	Register	Write *nnnnn* registers at address *yyyyy*	010*n nnnn* (40h+000*n nnnn*)	000*y yyyy* (00h+000*y yyyy*)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

14.5.1.1. SDATAC: Stop Read-data-continuous Mode

Conflicts may happen in the read-data-continuous mode when conversion data and register data are simultaneously giving out on DOUT by RDATA or RREG commands. Therefore, a SDATAC command is necessary to stop read-data-continuous mode before sending RREG or RDATA commands. Switching $\overline{CS}$ high cancels SDATAC status, so keep $\overline{CS}$ low to remain in SDATAC status.

14.5.1.2. WAKEUP: Recover from Standby Mode

WAKEUP command recovers the device from standby mode. There is no effect sending this command during normal operation.

14.5.1.3. STANDBY: Enter Standby Mode

STANDBY command makes the device enter a power-saving standby mode. In this mode, registers settings are saved and serial interface remains active. The device quits the standby mode by taking $\overline{CS}$ high or receiving WAKEUP command. To shut down the device completely, assert the $\overline{PWDN}$.

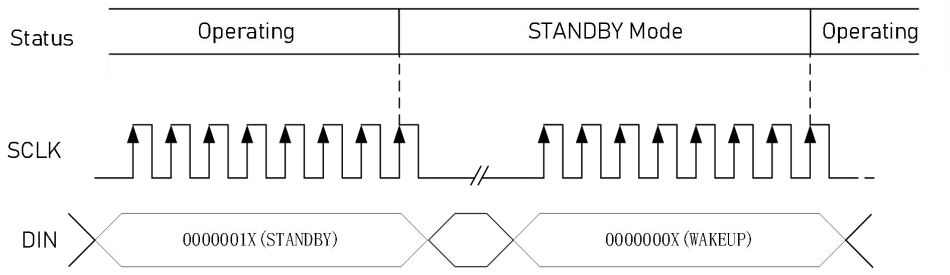

Fig. 33 STANDBY and WAKEUP Sequence

14.5.1.4. SYNC: Synchronize the AD Conversion

Once receiving the command, the reading in progress is canceled and the conversion is restarted. This can be used for synchronizing multiple LTD2284 by simultaneously sending the SYNC command. The SYNC pin needs to be kept logic high.

14.5.1.5. RESET: Reset the Device

This command rewrites all the registers to their default values and enters read-data-continuous mode. This is equivalent to asserting $\overline{\text{RESET}}$ pin.

14.5.1.6. RDATAC: Read Data Continuous

The device enters read-data-continuous mode, where manual read command is not needed. $\overline{\text{DRDY}}$ acts as an indicator to notify the user when data is read to read.

14.5.1.7. SDATAC: Stop Read Data Continuous

The device quits read-data-continuous mode upon receiving this command. Take $\overline{\text{CS}}$ high to cancel SDATAC status.

14.5.1.8. RDATA: Read Data by Command

Manually read the converted data by command. Read-data-continuous must be stopped first.

14.5.1.9. RREG: Read Register Data

This command consists of two bytes of code. First command byte states the starting address of desired registers to be read from. The next command byte states the number of registers to be read.A delay of 24 f_{CLK} cycles is required between each byte transaction. Following figure shows an example to read six registers starting from 05h.

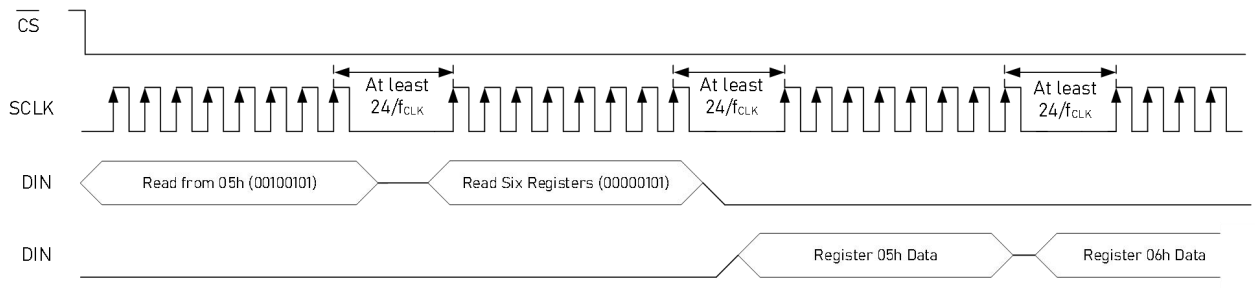

Fig. 34 RREG Sequence

14.5.1.10. WREG: Write Register Data

This command is for writing the registers. This command consists of two bytes of code followed by register data. First command byte states the starting address of desired registers to be written to. The next command byte states the number of registers to be read.A delay of 24 f_{CLK} cycles is required between each byte transaction. Following figure shows an example to write six registers starting from 05h.

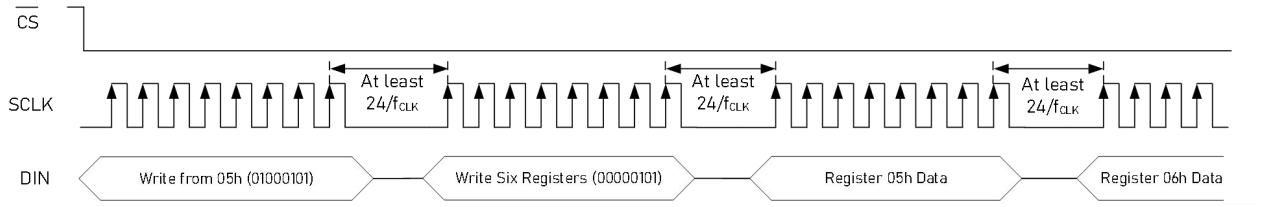

Fig. 35 WREG Sequence

14.5.1.11. OFSCAL: Offset Calibration

See session 14.2.12.

14.5.1.12. GANCAL: Gain Calibration

See session 14.2.12.

14.6. Register Map

By accessing and writing into the registers, the users can obtain all the information of the device, and thoroughly handle device. After any register has been rewritten, the device resets resulting in an interruption of 63 readings.

Table 15 Register Map

Addr.	Name	Default value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	ID_CFG	X0h	ID3	ID2	ID1	ID0	0	0	OFFSET1	OFFSET0
01h	CONFIG0	52h	SYNC	MODE	DR2	DR1	DR0	PHASE	FILTR1	FILTR0
02h	CONFIG1	08h	0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

14.6.1. Register Description

14.6.1.1. ID_CFG: ID_Configuration Register (address = 00h) [default =x0h]

ID_CFG Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	0	0	OFFSET1	OFFSET0
R-xh	R-xh	R-xh	R-xh	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

Bit[7:4] **ID[3:0]**
Factory-programmed identification bits (read-only). The ID bits are subject to change without notification.

Bit[3:2] **Reserved**
Always write 00

Bit[1:0] **OFFSET[1:0] (see Offset section)**
00: Offset disabled (default)

01: Reserved
10: Offset = 100/PGA mV
11: Offset = 75/PGA mV

14.6.1.2. CONFIG0: Configuration Register 0 (address = 01h) [default =52h]

CONFIG0 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC	MODE	DR2	DR1	DR0	PHASE	FILTR1	FILTR0
R/W-0h	R/W-1h	RW-0h	R/M-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

Bit[7] **SYNC**
Synchronization mode bit.
0: Pulse-sync mode (default)
1: Continuous-sync mode

Bit[6] **MODE**
Mode Control
0: Low-power mode
1: High-resolution mode (default)

Bit[5:3] **DR[2:0]**
Data rate select bits.
000: 250 SPS
001: 500 SPS
010: 1000 SPS (default)
011: 2000 SPS
100: 4000 SPS

Bit[2] **PHASE**
FIR phase response bit.
0: Linear phase (default)
1: Minimum phase

Bit[1:0] **FILTR[1:0]**
Digital filter configuration bits.
00: Reserved
01: Sinc filter block only
10: Sinc + LPF filter blocks (default)
11: Sinc + LPF + HPF filter blocks

14.6.1.3. CONFIG1: Configuration Register 1 (address = 02h) [default=08h]

CONFIG1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

Bit[7] **Reserved**
Always write 0

Bit[6:4] **MUX [2:0]**
MUX select bits.
000: AINP1 and AINN1 (default)
001: AINP2 and AINN2
010: Internal short through 400-Ω resistor
011: AINP1 and AINN1 connected to AINP2 and AINN2
100: External short to AINN2

Bit[3] **CHOP**
PGA chopping enable bit.
0: PGA chopping disabled
1: PGA chopping enabled (default)

Bit[2:0]

PGA[2:0]
PGA gain select bits.
000: G = 1 (default)
001: G = 2
010: G = 4
011: G = 8
100: G = 16
101: G = 32
110: G = 64

14.6.1.4. HPF0: High-pass Filter Corner Frequency, Low Byte (address = 03h) [default =32h]

HPF0 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.5. HPF1: High-pass Filter Corner Frequency, High Byte (address = 04h) [default =03h]

HPF1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	1R/W-1h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.6. OFC0: Offset Calibration, Low Byte (address = 05h) [default =00h]

OFC0 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.7. OFC1: Offset Calibration, Mid Byte (address = 06h) [default =00h]

OFC1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.8. OFC2: Offset Calibration, High Byte (address = 07h) [default =00h]

OFC2 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.9. FSC0: Full-scale Calibration, Low Byte (address = 08h) [default =00h]

FSC0 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.10. FSC1: Full-scale Calibration, Mid Byte (address = 09h) [default =00h]

FSC1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

14.6.1.11. FSC2: Full-scale Calibration, High Byte (address = 0Ah) [default =00h]

FSC2 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

R/W: Read/Write; R: Read only; -n = default value

15. Package Outlines

QFN5*4-24L

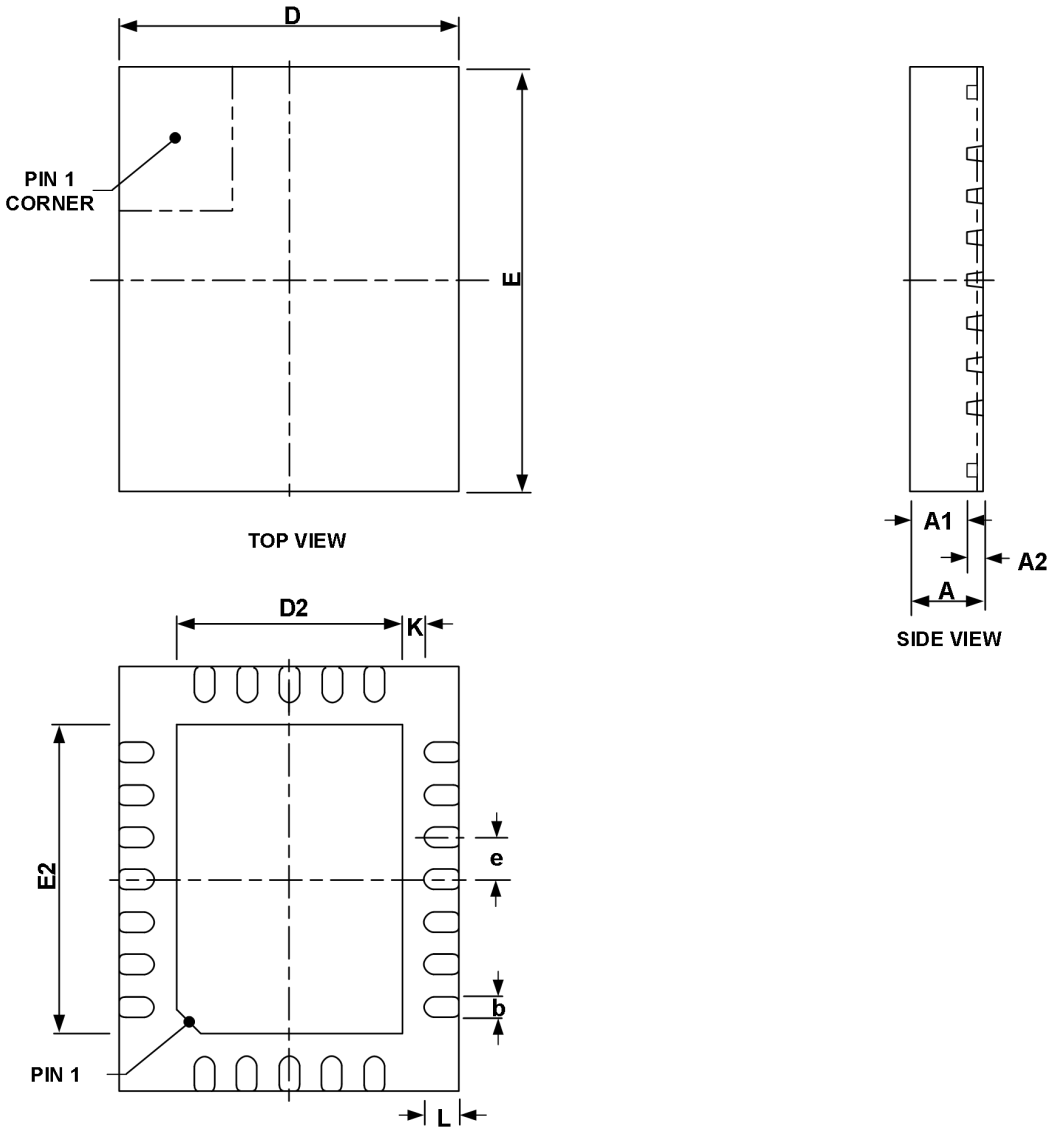

Table 16 Package Outlines			
Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	---	0.65	---
A2		0.203 REF	
b	0.2	0.25	0.3
D		4 BSC	
E		5 BSC	
e		0.5 BSC	
D2	2.55	2.65	2.75
E2	3.55	3.65	3.75
L	0.3	0.4	0.5
K		0.275 REF	